IPnexus™

ZT 5515*e*

Compute Processor Board

User's and System Integrator's Guide

PERFORMANCE
TECHNOLOGIES

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Errors and Omissions

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Performance Technologies, Inc., reserves its right to change product specifications without notice.

Symbols and Conventions in this Manual

The following symbols appear in this document:

Caution: There is risk of equipment damage. Follow the instructions.

Warning: Hazardous voltages are present. To reduce the risk of electrical shock and danger to personal health, follow the instructions.

Electrostatic Discharge

Caution: Electronic components on printed circuit boards are extremely sensitive to static electricity. Ordinary amounts of static electricity generated by your clothing or work environment can damage the electronic equipment. It is recommended that anti-static ground straps and anti-static mats are used when installing the board in a system to help prevent damage due to electrostatic discharge.

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Section
1 Introduction

This section provides an introduction to the Performance Technologies IPnexus™ ZT 5515*e* Compute Processor Board including a product definition, a list of product features, and a functional block diagram with descriptions of each block.

Figure 1, "ZT 5515*e* Faceplate" identifies the connectors, indicators, and switches available on the ZT 5515*e*'s faceplate. Optional rear-panel transition boards are available to extend various faceplate features to a system's rear-panel. For more information about compatible rear panel transition boards (RTM), see the *IPnexus ZT 4807e Packet Switched Rear-Panel Transition Board Hardware Manual*.

1.1 Product Definition

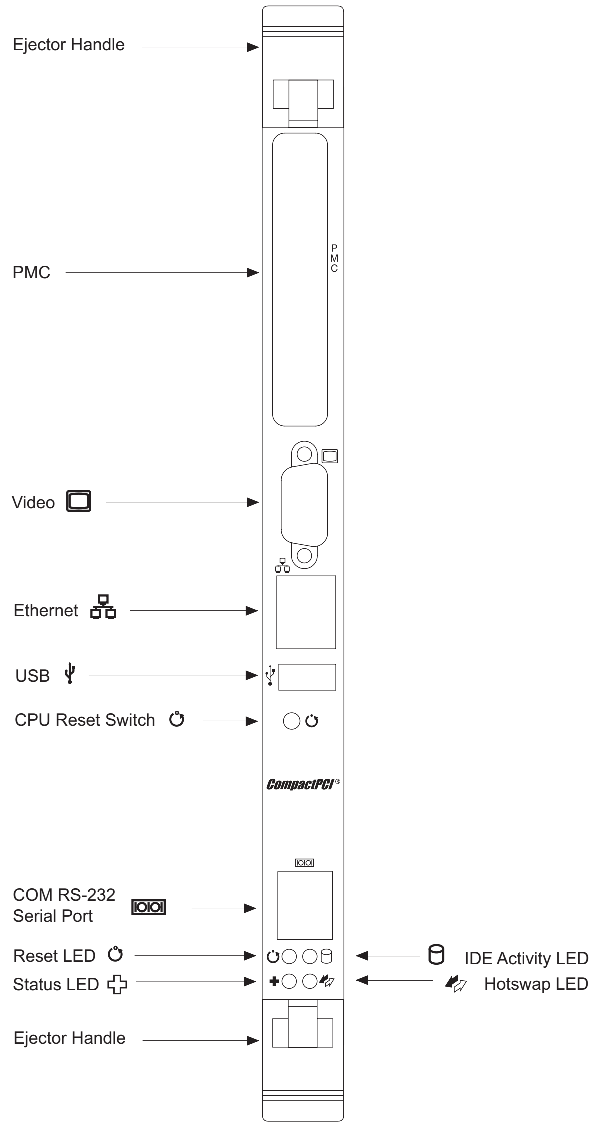
The ZT 5515*e* Compute Processor Board is a single board computer designed to work as a modular component in a CompactPCI® system. It utilizes the Mobile Intel® Pentium® 4 Processor -M in a micro FCPGA package along with dual Gigabit Ethernet controller and the latest in memory and I/O technology to provide an inexpensive, fast and reliable PICMG® 2.16 board. The ZT 5515*e* is CompactPCI Packet Switching Backplane (CompactPCI/PSB) compatible and draws its power from the J1 and J2 connectors, but it does not contain a CompactPCI bus. The ZT 5515e does include a dual Intelligent Platform Management Bus (IPMB) for system management along with IPMI v1.5 compatible firmware.

The ZT 5515*e* occupies a single 6U high Eurocard slot. The board can be used in either a system master slot or in a peripheral slot. In either case the ZT 5515*e* does not run or interact with other devices on the CompactPCI bus; instead this board relies on its fast Ethernet controller for interboard communications.

Although the ZT 5515*e* is highly integrated, its capabilities can be extended with optional boards available from Performance Technologies. Expansion boards are available to add CompactFlash® (ZT 96080) in place of the hard drive. Rear transition boards (IPnexus ZT 4807e) are available to extend I/O access to the rear of a system. For more information about options and accessories, see the Performance Technologies Web site at:

http://www.pt.com

Figure 1. ZT 5515*e* Faceplate



1.2 Features

There are two versions of the ZT 5515*e*. The first is the ZT 5515*e*A-1A, which has a PMC site and no on-board hard disk drive. The second is the ZT 5515*e*B-1A, which has an IDE connector and hard drive, but no PMC site. Both boards also feature 16 MB of on-board flash so an operating system such as VxWorks® could be loaded in the flash device. Other features include:

- CompactPCI Specification, PICMG 2.0, Version 2.1 compliant (see "CompactPCI" in Section 13, "Datasheet Reference")

  NOTE: There is no CompactPCI bus on this board, connectors J1 and J2 are used for Power and other signaling such as IPMI

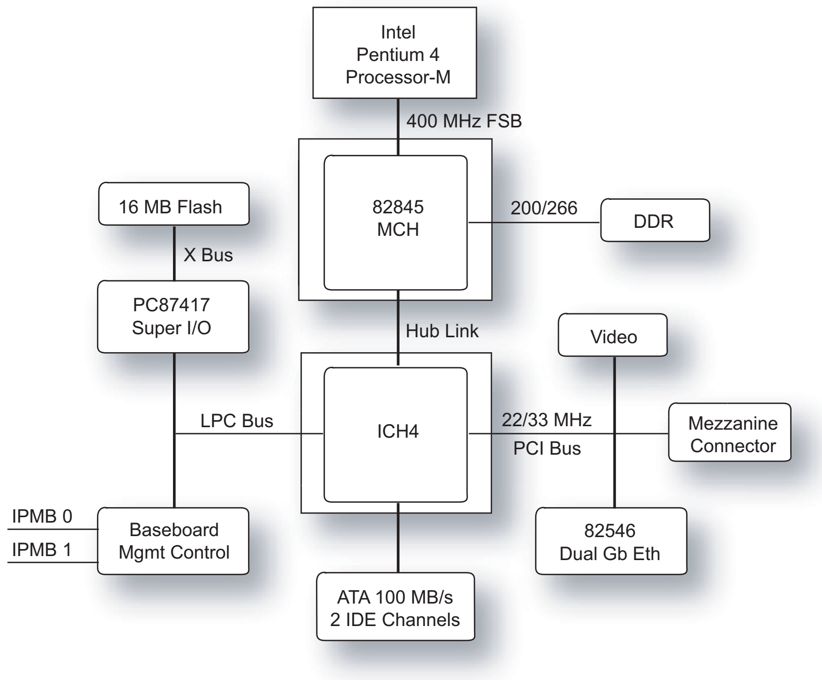
- CompactPCI Specification, PICMG 2.16, Version 1.0 compliant (see "CompactPCI" in Section 13)

- 6U single-slot CompactPCI form factor
- Mobile Intel Pentium 4 Processor - M, micro FCPGA package
- Intel 82845E MHC and ICH4
- Dual 10/100/1000 Mb/s Ethernet (one available at the faceplate or both at the J3 backplane connector)
- 512 KB of Level 2 cache
- 400 MHz front side bus
- Socketed 256 MB, 512 MB, or 1 GB of DDR SDRAM memory at 200 or 266 MHz
- 16 MB of on-board flash memory
- Dual stage watchdog timer
- Silicon Motion® LynxEM+® on-board video
- IPMI v2.0 firmware available through an Intel Baseboard Management Controller (BMC) chip
- Option for either a single on-board PCI Mezzanine Card (PMC) slot (32-bit / 33 MHz @ 3.3 V) or a primary IDE channel that supports an on-board 2.5 inch hard disk
- Two 16C550 RS-232 serial ports (COM1 available at the faceplate, COM1 and COM2 available through the J5 backplane connector)
- Push Button Reset on the front panel
- One USB port on front panel, two USB ports available via RTM
- Rear-Panel I/O availability (at J5) includes the following:
  - Secondary IDE channel
  - Floppy disk drive
  - Rear panel eject
  - Push-button reset
  - Two USB ports
- Support for Monta Vista® Linux®, Windows® .Net Server®, Windows 2000 Server, and VxWorks Tornado II®
- Standard AT® Systems include:
  - Two enhanced interrupt controllers (8259)
  - Three counter/timers (one 8254)
  - Real-time clock/CMOS RAM (146818B)
  - Two enhanced DMA controllers (8237)
  - 8042A compatible keyboard controller
  - PS/2 mouse and keyboard

1.3 Functional Blocks

The block diagram below shows basic features of the ZT 5515*e*. The following sections provide more detail on the features of the ZT 5515*e*.

Figure 2. Functional Block Diagram



CompactPCI/PSB Architecture

The ZT 5515*e* is designed to operate in a CompactPCI Packet Switching Backplane system (CompactPCI/PSB) though the board does not contain a CompactPCI bus. This allows the ZT 5515*e* to be used in any system master or peripheral slot of a PICMG 2.0 compliant chassis without interfering with the CompactPCI bus. The ZT 5515*e* uses only the J1 and J2 connectors for power and IPMI signaling.

When used in accordance with the *CompactPCI Packet Switching Backplane Specification, PICMG 2.16, Version 1.0*, the ZT 5515*e* functions as a "Dual Link Port Node" board. The ZT 5515*e* can be connected to a system's switching fabric by dual on-board Ethernet connections, and can be inserted into system or peripheral slots. The ZT 5515*e* is keyed for insertion into compatible slots.

The "CompactPCI" topic in Section 13 contains a link to the PCI Industrial Computer Manufacturers Group, from whom CompactPCI specifications can be purchased.

Processor

The ZT 5515*e* uses the Mobile Intel Pentium 4 Processor - M in a micro FCPGA package. The FCPGA package is a highly integrated assembly containing the processor and its immediate system-level support. This mobile processor runs at a lower voltage than the desktop version.

The 512 KB on-die transfer L2 cache is integrated with the CPU, eliminating the need for separate components and improving performance. The FCPGA package Pentium 4 processor also operates with a 400 MHz Processor Side Bus for fast access to memory and data.

The "Mobile Intel Pentium 4 Processor - M (FCPGA Package)" topic in Section 13 contains a link to the datasheet for the processor.

Chipset

The Intel 845E chipset consists of two controller hubs: the 82845E Memory Controller Hub (MCH) supports a 400MHz or 533MHz system bus, DDR200/266 memory and the latest graphics devices through the 1.5 V AGP4X interface. The 82801DB I/O Controller Hub (ICH4) makes a direct connection to the graphics and memory for faster access to peripherals. It provides the features and bandwidth required for applied computing-usage models. The following is a list of features of the 845E chipset:

- Designed, validated, and optimized for the Intel Pentium 4 Processor and Mobile Intel Pentium 4 Processor - M with Intel NetBurst™ micro-architecture using proven and established building blocks
- 400MHz or 533MHz system bus delivers a high-bandwidth connection between the Intel Pentium 4 Processor and the platform, providing 3x the bandwidth over platforms based on Intel Pentium III Processors
- Three USB controllers provide high performance peripherals with 480 Mbps of bandwidth, while enabling support for up to six USB 2.0 ports. This results in a significant increase over previous integrated 1-4 port hubs at 12 Mbps.
- Dual Ultra ATA/100 controllers, coupled with the Intel Application Launch Accelerator - a performance software package - support faster IDE transfers to storage devices
- The Application Accelerator software provides additional performance over native ATA drivers. The Intel Application Accelerator improves system performance by improving I/O transfer rates and enables faster O/S load time resulting in accelerated boot times
- Embedded lifecycle support

The "Intel 845E Chipset" topic in Section 13 contains a link to information about the chipset.

PCI-to-PCI Bridge (Not supported)

The ZT 5515*e* does have an on-board PCI bus, but ***does not*** have a CompactPCI bridge to the backplane. The ZT 5515*e* still has the J1/J2 connectors in order to support other requirements for the board such as power and the IPMI bus.

Memory and I/O Addressing

The ZT 5515*e* supports 256 MB, 512 MB or 1 GB of socketed ECC DDR SDRAM memory. ECC will correct single bit errors (97 percent of all DRAM errors are single bit errors) and can report multiple bit errors to the operating system.

In addition to SDRAM, the ZT 5515*e* provides 16 MB of on-board flash memory. The system BIOS uses 1 MB of this flash, the other 15 MB are free for user configuration.

For more information, see "Memory Configuration" and "I/O Configuration" in Section 2, "Getting Started."

Power Ramp Circuitry

The ZT 5515*e* features a power controller with power ramp circuitry that allows the board's voltages to be ramped in a controlled fashion. The power ramp circuitry eliminates large voltage or current spikes caused by hot swapping boards. This controlled ramping is a requirement of the CompactPCI Hot Swap Specification, PICMG 2.1, Version 1.0 (see "CompactPCI" in Section 13).

The ZT 5515*e*'s power controller unconditionally resets the board when it detects that the 3.3V, 5V, and 12V supplies are below an acceptable operating limit. Minimum voltage thresholds for the ZT 5515*e* are: 4.75V (5V supply), 3.0V (3.3V supply), and 10.0V (+12V supply).

Fault current sensing is also provided. If a board fault (short circuit) or over-current condition is detected, the power controller removes power from the ZT 5515*e*'s components and the Health LED on the faceplate turns amber. Fault protection activates if the current exceeds the threshold for greater than 50µs. The ZT 5515*e*'s fault current limits are shown in the following table.

Table 1. Fault Current Limits

Power Source	Minimum	Maximum
+5.0V	10.0A	15.0A
+3.3V	9.4A	14.1A
+12V	1.0A	1.5A
-12V	0.6A	0.9A

NOTE: The fault trip currents listed above are design values. Noisy power sources can lower the fault trip current limits to less than the minimum design values.

NOTE: Over-current on the -12V supply does not activate the fault trip circuit breaker and the LED does not turn amber. -12V is over-current protected by a resettable (PTC) 0.75 A fuse.

Rear-Panel I/O

The following I/O signals are available from the J5 connector at the back of the ZT 5515*e* (see the "J5 Rear Panel I/O Connector Pinout" table in Section 4, "Connectors"). These signals are available for use by a RTM such as the ZT 4807*e*.

- Serial ports (COM1 and COM2)
- USB Ports 2 and 3
- Floppy Interface
- Keyboard
- PS/2 mouse
- Push button reset input
- Secondary IDE channel
- SMBus
- Ejector

- Video
- Speaker Output (AT compatible)

PCI Video

The ZT 5515*e* provides on-board video through a Silicon Motion LynxEM+ ultra low power video chip. This device is configured for PCI bus transactions at speeds up to 33 MHz.

The Lynx chip incorporates 2 MB of integrated SDRAM for the graphics/video frame buffer. Video signals are available at the ZT 5515*e*'s J25 faceplate connector or at the J5 Rear Panel I/O connector (see "J25 VGA Connector" and "J5 Rear Panel I/ O Connector Pinout" in Section 4).

See "SW3-4 (VGA Routing Control)" in Section 3, "Configuration," for information on directing video signals to the front or rear of the board.

The "Video" topic in Section 13 contains a link to the Web site for this device.

PCI Mezzanine Card (PMC) Interface

The ZT 5515*e*A-1A provides a location for one on-board PMC device with front panel access. The PMC interface is on PCI Bus 0 and uses a 32-bit 3.3V PCI bus. The ZT 5515*e*A-1A does not have a primary IDE connector on-board nor a hard drive. In contrast, the ZT 5515*e*B-1A does have an IDE connector and hard drive, but does not have a PMC site.

See "PMC Specification" in Section 13 for a link to the sponsoring organization for the PMC specification.

Dual Ethernet Interfaces

The ZT 5515*e* provides two 10/100/1000BaseTx Ethernet channels (ENETA and ENET B) through the Intel 82546EB Fast Gigabit Ethernet Multifunction PCI Controller. The 82546EB consists of both the Media Access Controller (MAC) and the physical layer (PHY) interface combined into a single component solution. One RJ-45 connector is available on the front panel faceplate and two Ethernet Channels can be directed to the rear connector at J3 (software selectable in the BIOS). See "Geographic Addressing (E4h)" in Section 12, "System Registers," for more information.

See "Ethernet" in Section 13 for links to the datasheets for the Ethernet devices used on the ZT 5515*e*.

IDE Hard Drive

The ZT 5515*e*A-1B includes an on-board 2.5-inch Enhanced IDE hard drive. The hard drive is on the ZT 5515*e*'s primary IDE channel and is assigned "device 0" (master) identity.

See Section 7, "IDE Controller," for more information.

Serial I/O

The ZT 5515*e* provides support for two RS-232 compatible serial ports. COM1 is accessible at the faceplate through an RJ-45 connector or through the J5 Rear Panel I/O connector. This port is typically used for test access. Both COM1 and COM2 are available at the J5 Rear Panel I/O connector. No strapping option or software control is required to use either port.

The front panel serial port is available via a RJ-45 connector and is configured as DTE. SRI (Serial Ring Indicator) and SCD (Serial Carrier Detect) signals are not included in the front panel RJ-45 connector. See "J30 COM1 Serial Port Pinout" in Section 4 for a connector pinout.

NOTE: COM1 signals are available to the front- and rear-panel simultaneously. Utilizing the COM1 signal at the front and rear at the same time will cause a signaling conflict.

The ZT 5515*e*'s serial controller resides in the National Semiconductor® PC87417 SuperI/O® device. See "SuperI/O" in Section 13 for a link to the datasheet for this device.

Interrupts

Two enhanced, 8259-style interrupt controllers provide the ZT 5515*e* with a total of 15 interrupt inputs. Interrupt controller features include support for:

- Level-triggered and edge-triggered inputs
- Individual input masking
- Fixed and rotating priorities

Interrupt sources include:

- Counter/Timers
- Serial I/O
- Keyboard
- Floppy disk
- IDE interface
- Real-Time Clock
- On-board PCI devices

Enhanced capabilities include the ability to configure each interrupt level for active high-going edge or active low-level inputs.

The ZT 5515*e*'s interrupt controllers reside in the ICH4 device.

See "Intel 845E Chipset" in Section 13 for a link to the datasheet for this device.

Counter/Timers

Three 8254-style counter/timers, as defined for the PC/AT, are included on the ZT 5515*e*. Operating modes supported by the counter/timers include:

- Interrupt on count
- Frequency divider
- Square wave generator
- Software triggered

- Hardware triggered
- One shot

The ZT 5515*e*'s Counter/Timers reside in the Intel ICH4 device.

See “Intel 845E Chipset” in Section 13 for a link to the datasheet for this device.

DMA

Two cascaded 8237-style DMA controllers are provided on the ZT 5515*e* for use by the on-board peripherals. The ZT 5515*e*'s DMA controllers reside in the Intel ICH4 device.

See “Intel 845E Chipset” in Section 13 for a link to the datasheet for this device.

Real-Time Clock

The real-time clock performs timekeeping functions and includes 256 bytes of general-purpose, battery-backed, CMOS RAM. Timekeeping features include an alarm function, a maskable periodic interrupt, and a 100-year calendar. The system BIOS uses a portion of this RAM for BIOS setup information.

The ZT 5515*e*'s Real-Time Clock resides in the Intel ICH4 device.

See “Intel 845E Chipset” in Section 13 for a link to the datasheet for this device.

Reset

The push-button reset on the ZT 5515*e*'s faceplate functions as a “Hard Reset.”

See Section 5, “Reset,” for more information about reset sources for the ZT 5515*e*.

Two-Stage Watchdog Timer

The watchdog timer optionally monitors system operation and is programmable for one of eight different timeout periods (from 0.25 seconds to 256 seconds). It is a two-stage watchdog, meaning that it can be enabled to produce a non-maskable interrupt (NMI) or a “CPU init” before it generates a Reset. Failure to strobe the watchdog timer within the programmed time period may result in an NMI, a reset request, or both. A register bit can be enabled to indicate if the watchdog timer caused the reset event. This watchdog timer register is cleared on power-up, enabling system software to take appropriate action if the watchdog generated the reboot.

See Section 7, “Watchdog Timer,” for more information, including sample code.

Universal Serial Bus (USB)

The Universal Serial Bus (USB) provides a common interface to slower-speed peripherals. Functions such as keyboard, serial ports, and mouse ports can be consolidated into USB, simplifying cabling requirements. The ZT 5515*e* provides one USB port at its faceplate (connector J20 is Port 0). USB Port 1 and USB port 2 are routed to the ZT 5515*e*'s J5 Rear Panel I/O connector. See “J5 Rear Panel I/O Connector Pinout” in Section 4.

The ZT 5515*e*’s USB channels are controlled by the Intel ICH4 device.

See "Intel 845E Chipset" in Section 13 for a link to the datasheet for this device.

Baseboard Management Controller

The ZT 5515*e* includes an Intel Baseboard Management Controller (BMC) chip, the VT22030A, which interfaces to the LPC bus. The BMC provides SMBus (System Management Bus) interfaces and is IPMI (Intelligent Platform Management Interface) compliant. The BMC subsystem monitors, controls, and performs remote diagnostics for on- and off-board functions.

See Section 6, "System Monitoring and Control" for more details.

IDE Controller

The ZT 5515*e*A-1B (but ***not*** the ZT 5515*e*A-1A) features an ATA-100 IDE connector and an onboard IDE drive. ATA-100, also called DMA-100, is an enhancement to earlier IDE standards that increases throughput to 100 MB/sec using Bus Master IDE transfers. Additionally, the controller can handle either 33, 66 or 100 MB/sec transfers depending on the drive installed.

The primary IDE channel signals are available through the J8 IDE connector (see "J8 (IDE Connector)" in Section 4). Secondary channel IDE signals are available through the J5 Rear Panel I/O connector (see "J5 (Rear Panel I/O CompactPCI Connector" in Section 4).

See Section 7, "IDE Controller," for more information on the ZT 5515*e*'s IDE controller.

The ZT 5515*e*'s IDE controller resides in the Intel ICH4 device. See "Intel 845E Chipset" in Section 13 for a link to the datasheet for this device.

Floppy Disk Controller

The ZT 5515*e* includes a 2.88 MB Super I/O Floppy Disk Controller that supports an optional external floppy drive through the PC87417 device. Floppy signals are available through the J5 Rear Panel I/O connector (see "J5 (Rear Panel I/O CompactPCI Connector" in Section 4).

See "SuperI/O" in Section 13 for a link to the datasheet for ZT 5515*e*'s I/O controller.

Keyboard and Mouse Controller

The ZT 5515*e* includes an on-board PC/AT keyboard controller. The ZT 5515*e* also includes an onboard PS/2-style mouse controller. There are no front PS/2 connectors. The keyboard and mouse signals are available through the J5 Rear Panel I/O connector (see "J5 (Rear Panel I/O CompactPCI Connector" in Section 4).

See "SuperI/O" in Section 13 for a link to the datasheet for ZT 5515*e*'s I/O controller.

LED Indicators

The LEDs located at the ZT 5515*e*'s faceplate are defined below.

- Ethernet (ENETA, RJ 45 connector)
  - First bi-colored LED:

    Green = Network connection
    Blinking Green = Network activity

  - Second bi-colored LED:
    Off = 10 MB/sec
    Green = 100 MB
    Yellow = 1000 MB
- IDE Activity (Disk 0 and Disk 1)
  - Green = disk activity
- Hot Swap
  - Blue = safe to extract board
  - Off = not safe to extract board
- Reset Status
  - Green = Normal operation
  - Red = In reset
- Health
  - Green = normal operation
  - Amber = needs attention

1.4 Software

The ZT 5515*e* includes an AMI® Embedded BIOS loaded in on-board flash. The BIOS is user configurable and can boot an operating system from local flash memory, CompactFlash, a hard drive, CD-ROM drive, or over a network. BIOS and firmware updates can be downloaded from the Performance Technologies Web site.

The ZT 5515*e* is compatible with all major PC operating systems, including Microsoft® Windows 2000, Linux, and VxWorks. Performance Technologies may provide additional drivers for peripherals, flash drives, and for supported operating systems. Software device drivers for the ZT 5515*e* can be found on the Performance Technologies Web site.

Section
2 Getting Started

This section summarizes the information needed to make the ZT 5515*e* operational. Please read this section before using the board.

2.1 Unpacking

Check the shipping carton for damage. If the shipping carton and contents are damaged, notify Performance Technologies Customer Support. Retain the shipping carton and packing material for inspection by the carrier. Obtain authorization before returning any product to Performance Technologies.

Refer to Section 15, "In Case of Difficulty" for assistance information.

NOTE: This board must be protected from static discharge and physical shock. Never remove any of the socketed parts except at a static-free workstation. Use the anti-static bag shipped with the product to handle the board. Wear a wrist strap grounded through one of the system's ESD Ground jacks when servicing system components.

2.2 System Requirements

The following topics briefly describe the basic system requirements and configurable features of the ZT 5515*e*. Links are provided to other sections containing more detailed information.

BIOS Version

For proper operation, the ZT 5515*e* must run the Performance Technologies Embedded BIOS (AMI CORE), revision C01 or P01 and later (P01-Pxx). The revision level is shown in the BIOS Identification string displayed during the Power On Self Test (POST). The revision level is the fourth field in the BIOS ID string. For more information, see the *Performance Technologies Embedded BIOS Manual*.

Connectivity

The ZT 5515*e* has no bridge chip and therefore has no CompactPCI signaling on its J1and J2 connectors. The connectors are only on the board for power and IPMI signaling.

The ZT 5515*e* features an ejector handle that is keyed for compatible slots. The board can only be inserted into slots fitted with a compatible mating key.

The ZT 5515*e* is designed to operate in a backplane providing CompactPCI form factor interfaces at J1, J2, J3, and J5. The J1 and J2 connectors are supplied for power and IPMI signals. J3 signaling must comply with the PICMG 2.16 Packet Switching Backplane specification. The J5 interface must have through-pins for the ZT 5515*e* to interface with an RTM such as the ZT 4807*e*.

See Section 4, "Connectors" for connector descriptions.

Electrical and Environmental

The ZT 5515*e* meets the following requirements:

- +5V DC +5%, -3% @ 4.5 A typical
- +3.3 VDC +5%, -3% @ 2.5 A typical
- +12 VDC ±10% @ 20 mA typical
- -12 VDC may be required by a PMC peripheral installed on the ZT 5515*e*.

Table 2. Electrical and Environmental

Configuration	5V (avg)	5V (peak)	3.3V (avg)	3.3V (peak)	12V (avg)	12V (peak)	-12V (avg)	-12V (peak)
1.2 GHz / 512 MB	4.5 A	TBD[3]	2.5 A	TBD[3]	20 mA	50 mA	0.0 A	0.0 A
Hard disk (add) (typical)	540 mA	1.00 A	N/A	N/A	N/A	N/A	N/A	N/A
PMC card typical[1] (add)	1.00 A	1.70 A	0.75 A	1.30 A	100 mA	200 mA	20 mA	40 mA
PMC card max.[2] (add)	1.50 A	3.00 A	2.25 A	4.50 A	500 mA	500 mA	500 mA	500 mA

NOTES:
1. Consult manufacturer of installed PMC card for actual values.
2. In no case shall the total power dissipated by the PMC card exceed 10.0 W.
3. Peak (short duration) power supply current may be significantly higher (up to 50%) and will vary depending upon the application.

The ZT 5515*e* does not correctly terminate the PCI bus if used in a system master slot since it has no CompactPCI bus. If you are planning on using the CompactPCI bus then you should use a board that is a CompactPCI master, such as the IPnexus ZT 5504*e* System Master Processor Board, in the system master slot.

The ZT 5515*e* comes with a heat sink that allows the processor to operate between 0° and approximately 50° C ambient with a minimum of 200 LFM (1 meter per second) of external airflow. It is the user's responsibility to ensure that the ZT 5515*e* is installed in a chassis capable of supplying adequate airflow. The maximum power dissipation of the processor (FCPGA package) is 25 W. External airflow **must** be provided at all times.

See Section 10, "Specifications," and Section 11, "Thermal Considerations," for more details.

It is strongly recommended that the airflow be measured while the ZT 5515*e* is installed in its intended location. Insert a thermistor type air velocity meter (Kane-May KM4007 or similar) through the PMC access on the faceplate and make the air velocity measurement near the processor heat sink. Power should not be applied to the ZT 5515*e* during airflow measurements (slightly disengage the ZT 5515*e* from the backplane connectors if necessary).

Warning: The processor "core" temperature must never exceed 100° C under any condition of ambient temperature or usage. This can result in permanent damage to the processor.

The ZT 5515*e* may contain materials that require regulation upon disposal. Please dispose of this product in accordance with local rules and regulations. For disposal or recycling information, please contact your local authorities or the Electronic Industries Alliance at http://www.eiae.org/.

2.3 Memory Configuration

The ZT 5515*e* components can *address* up to 4 GB of memory, but since the board has only one DIMM socket it can physically hold up to 1 GB of memory. The address space is divided between memory local to the board and memory located on the Local PCI bus. Any memory not reserved or occupied by a local memory device (DRAM/flash) is available to PCI memory devices.

The ZT 5515*e* can support a single stick of either 256 MB, 512 MB or 1 GB ECC DDR SDRAM in a single 90° angle DIMM socket. 512 KB of L2 cache is integrated with the Mobile Pentium 4 Processor - M.

16 MB of local flash memory is soldered directly to the board and is divided into 128 128-KB erase blocks. The on-board BIOS is stored in the first 1 MB of this local flash. The rest is open for customer use. For example, a VxWorks operating system could be loaded into the upper 15 MB and could be used as a boot device.

The “Memory Address Map Example” figure shows example memory addressing for the ZT 5515*e*.

Figure 3. Memory Address Map Example

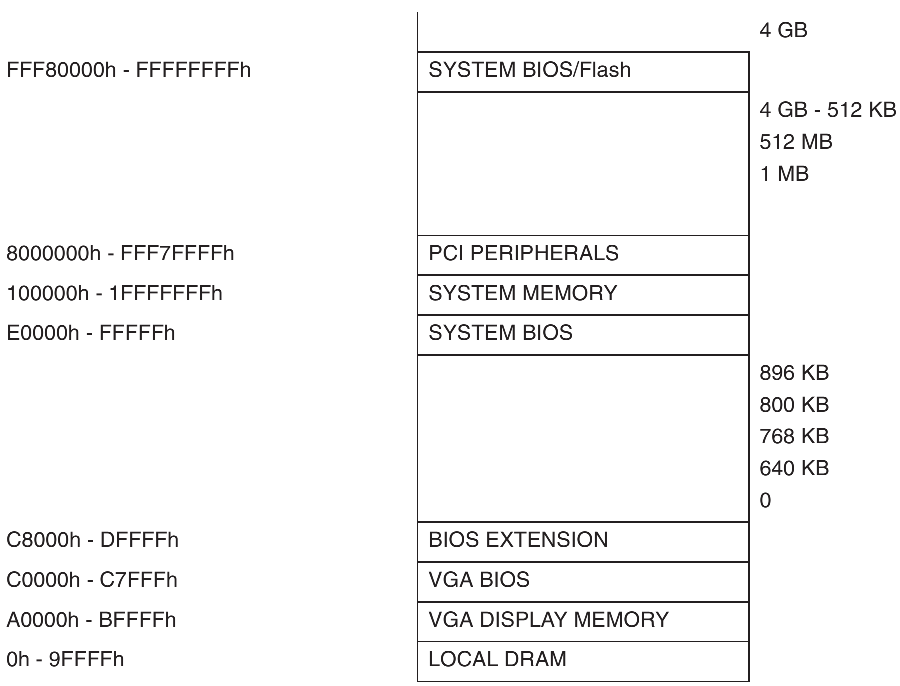


Figure 4. I/O Address Map

*Onboard ISA peripherals addressed between 100h - 7FFh decode 11 bits of address (A0h - A10h). Therefore, these peripherals will alias throughout the 16-bit I/O space at the following ranges:
x100-x3FFh
x500-x7FFh
x900-xBFFh
xD00-xFFFh
PCI devices can fully utilize the address space from D00 - FFFFh, since subtractive decoding is used for the onboard ISA devices.

D00 - FFFFh	PCI*
CF8 - CFFh	PCI Config/RST Control
780 - CF7h	PCI Reserved
778 - 77Fh	LPT ECP Registers
400 - 777h	Reserved
3F8 - 3FFh	COM1
3F0 - 3F7h	Floppy / IDE Registers
3E0 - 3EFh	Reserved
3B0 - 3DFh	VGA Registers
380 - 3AFh	Reserved
378 - 37Fh	LPT
300 - 377h	Reserved
2F8 - 2FFh	COM2
200 - 2F7h	Reserved
1F8 - 1FFh	Reserved
1F0 - 1F7h	Primary IDE Registers
178 - 1DFh	Reserved
170 - 177h	Secondary IDE Registers
100 - 16Fh	Reserved
F0 - FFh	Coprocessor
E6 - EFh	Reserved
E1 - E5h	ZT 5515 System Registers 1-5
E0Fh	Reserved
C0 - DFh	On-board Slave DMA Controller
B4 - BFh	Reserved
B2 - B3h	APM Registers
B0 - B1h	Reserved
A0 - AFh	On-board Slave Interrupt Controller
93 - 9Fh	Reserved
92h	Fast RESET and Gate A20
90 - 91h	Reserved
81 - 8Fh	On-board DMA Page Registers
80h	Diagnostic Port
79h	Board's Watchdog Timer Register
78h	Board's System Register 0
70 - 77h	On-board Real-Time Clock
60 - 6Fh	Keyboard and System Ports
50 - 5Fh	Reserved
40 - 4Fh	On-board Timer/Counters
30 - 3Fh	Reserved
2E - 2Fh	87309 Super I/O Configuration
22 - 2Dh	Reserved
20 - 21h	On-board master Interrupt Controller
0 - 1Fh	On-board Master DMA Controller

2.4 I/O Configuration

The ZT 5515*e* addresses up to 64 KB of I/O using a 16-bit I/O address. The ZT 5515*e* is populated with many commonly used I/O peripheral devices. The I/O address location for each peripheral is shown in Figure 4, "I/O Address Map," above.

2.5 Connectors

The ZT 5515*e* includes several connectors to interface to application-specific devices. Refer to Section 4 "Connectors" for complete connector descriptions and pinouts.

2.6 Switch Options

The ZT 5515*e* provides several switch configuration options for features that cannot be provided through the BIOS Setup utility. Location figures and descriptions are provided in Section 3, "Configuration."

2.7 BIOS Configuration Overview

This topic presents an introduction to the ZT 5515*e*'s BIOS. For more detailed information about the BIOS and other utilities, see the *Performance Technologies Embedded BIOS Manual* available on the Performance Technologies Web site.

The BIOS has many separately configurable features. These features are selected by running the built-in Setup utility. System configuration settings are saved in a portion of battery-backed RAM in the real-time clock device and are used by the BIOS to initialize the system at boot-up or reset. The configuration is protected by a checksum word for system integrity.

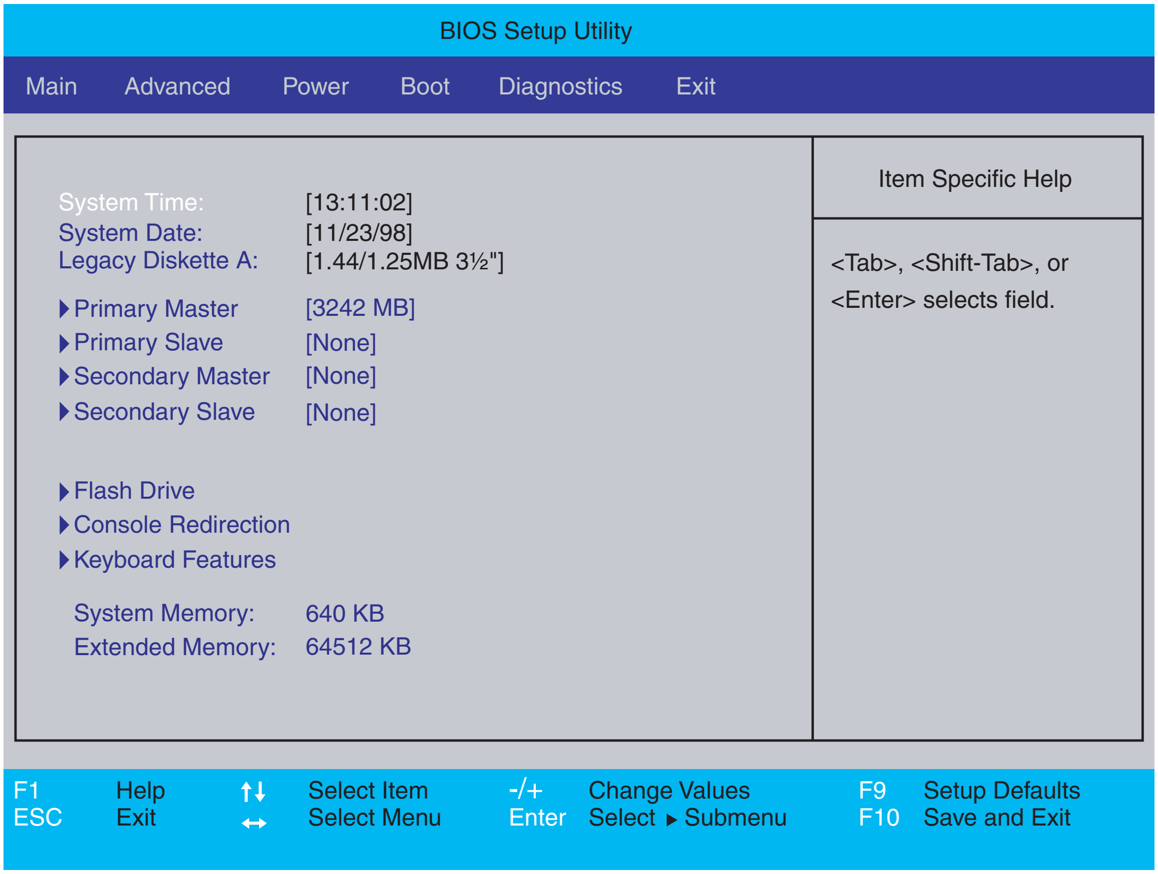
To access the Setup utility, press **F2** during the system RAM check at boot-up. When Setup runs, an interactive configuration screen displays. Refer to Figure 5, "Setup Screen" for an example.

Setup parameters are divided into different categories. The available categories are listed in a menu across the top of the Setup screen. The parameters within the highlighted (current) category are listed in the main (left) portion of the Setup screen. Context sensitive help is displayed in the right portion of the screen for each parameter. A legend of keys is listed at the bottom of the Setup screen.

Use the left and right arrow keys to select a category from the menu. Use the up and down arrow keys to select a parameter in the main portion of the screen. Use the **+** or – keys to change the value of a parameter.

Solid arrows next to menu items in the main screen indicate submenus. To display a submenu, use the up and down arrow keys to highlight the submenu and then press **Enter**.

Figure 5. Setup Screen



2.8 Operating System Installation

For more detailed information about your operating system, refer to the documentation provided by the operating system vendor.

1. Install peripheral devices. CompactPCI devices are automatically configured by the BIOS during the boot sequence.
2. Most operating systems require initial installation on a hard drive from a floppy or CD-ROM drive. These devices should be configured, installed, and tested with the supplied drivers before attempting to load the new operating system.
3. Read the release notes and installation documentation provided by the operating system vendor. Be sure to read any README files or documents provided on the distribution disks, as these typically note documentation discrepancies or compatibility problems.
4. Select the appropriate boot device order in the SETUP boot menu depending on the OS installation media used. For example, if the OS includes a bootable installation floppy, select **Removable Media** as the first boot device and reboot the system with the installation floppy installed in the floppy drive.

   NOTE: If the installation requires a non-bootable CD-ROM, it is necessary to boot an OS with the proper CD-ROM drivers in order to access the CD-ROM drive.

5. Proceed with the OS installation as directed, being sure to select appropriate device types if prompted. Refer to the appropriate hardware manuals for specific device types and compatibility modes of Performance Technologies products.
6. When installation is complete, reboot the system and set the boot device order in the SETUP boot menu appropriately.
7. The Flash Write Protect/Write Enable switch, SW2-1, must be open when installing an operating system image into flash. See "SW2-1 (Flash Write-Protect)" in Section 3 for more information.

Section

3 Configuration

The ZT 5515*e* has been designed for maximum flexibility. Many features can be configured by the user for specific applications. Most configuration options are selected through the BIOS Setup utility (discussed in "BIOS Configuration Overview" in Section 2). Some options cannot be software controlled and are configured with switches. Switch options are made by closing or opening the appropriate switch.

3.1 Switch Options and Locations

The ZT 5515*e* contains a push-button switch on the faceplate and three banks of DIP switches on the component side of the board. The switches are listed and briefly described in the "Switch Cross- Reference" table below.

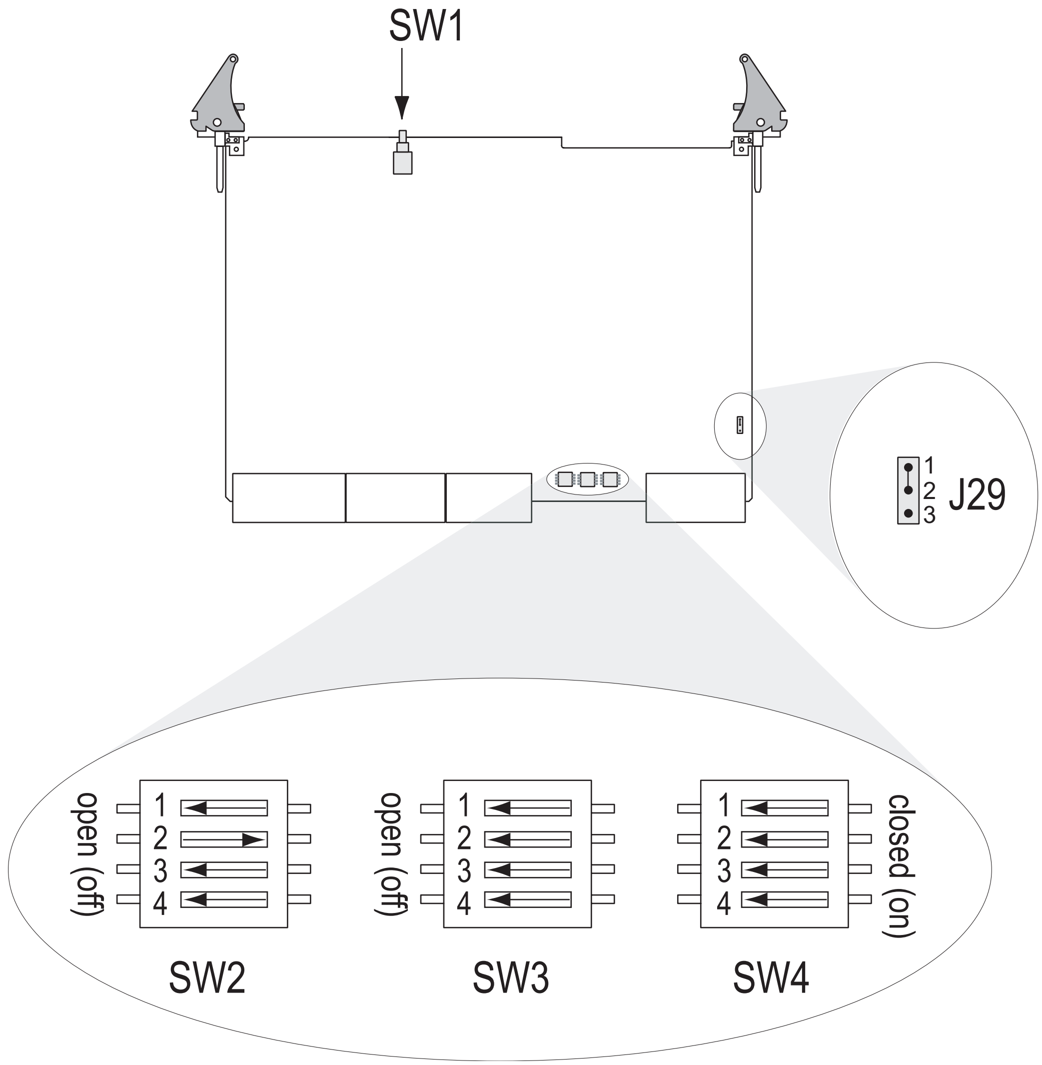
Factory default switch settings are shown in Figure 6, "Default Switch Configuration."

NOTE: Where switches are referenced in this section, "SWX" refers to the switch number and "-N" refers to the switch segment (SW4-2 means "switch number 4, segment 2").

Table 3. Switch Cross-Reference Table

Switch	Function
SW1	Reset (push-button on faceplate)
SW2-1	BIOS flash write protect
SW2-2	Baseboard Management Controller write protect
SW2-3	Real Time Clock reset
SW2-4	CMOS Clear
SW3-1	BIOS Recovery Module/Flash Select
SW3-2	Bypass BMC to power up
SW3-3	Ethernet SMBUS Isolation
SW3-4	VGA routing (front / back)
SW4-1	User Software Configuration 0
SW4-2	User Software Configuration 1
SW4-3	Console Redirection
SW4-4	BMC dual domain mode
SW5	Ejector

Figure 6. Default Switch Configuration



3.2 Switch Descriptions

The following topics list the switches in numerical order and provide a detailed description of each switch.

SW1 (Reset)

SW1 is a push-button on the front of the ZT 5515*e*. Pressing SW1 issues a hard reset. Reset is discussed in more detail in Section 5, "Reset."

SW2-1 (Flash Write-Protect)

Closing this switch write-protects flash memory. Open SW2-1 when installing an operating system image (such as VxWorks) into flash or when using the FLASH.EXE utility to recover from a corrupted BIOS or update the BIOS. The status of this switch can be read back at the

Switch Monitor register (Port E3h, bit 7). Factory default is open (not write protected). See "Switch Monitors (E3h)" in Section 12 for the Switch Monitor Register (E3h) definition.

SW2-1		Function
Open	Default	BIOS (on-board flash) read/write.
Closed		BIOS (on-board flash) is write protected (read only).

SW2-2 (IPMI Flash Write Protect)

Closing this switch write-protects the IPMI firmware flash memory. Opening the switch allows IPMI firmware updates. This switch must be open when using an update utility.

SW2-2		Function
Open		Flash firmware read/write.
Closed	Default	Flash firmware write protected (read only).

SW2-3 (Real-Time Clock Reset)

Closing this switch clears the CMOS real-time clock.

SW2-3		CMOS Real Time Clock
Open	Default	Normal Operation
Closed		Real Time Clock Reset

SW2-4 (CMOS Clear)

Closing this switch clears the system CMOS. This switch is connected to GPIO35 of ICH4.

SW2-4		CMOS Real Time Clock
Open	Default	Normal Operation
Closed		Clear CMOS

SW3-1 (BIOS Recovery Module/Flash Select)

If your system is having trouble booting then you may want to try using this switch to boot from the backup BIOS. When SW3-1 is open, the BIOS boots from the normal location of on-board flash memory. When SW3-1 is closed, the BIOS boots from the backup BIOS. See "On-board Flash Memory" in Section 9 for details on how to flash the BIOS.

SW3-1		**Function**
Open	Default	Boots from normal BIOS area
Closed		Boots from the backup BIOS

SW3-2 (Bypass BMC to Power Up)

If you are having difficulty powering up the ZT 5515*e* you may want to try closing this switch to bypass the BMC firmware and (possibly) allow the board to boot. This can be used if the BMC firmware on the board is not available. This switch should be closed when the board is used in a non-PICMG 2.9 chassis (i.e., a chassis that does not supply IPMB power) or when power up difficulties are encountered.

SW3-2		**Function**
Open	Default	BMC controls the board power up
Closed		BMC is bypassed during board power up

SW3-3 (Ethernet SMBUS Isolation)

Closing this switch disables the SMBUS connection from the BMC to the Ethernet. This is used to disable remote management.

SW3-3		**Function**
Open	Default	The SMBUS to Ethernet connection is *enabled*
Closed		The SMBUS to Ethernet connection is *disabled*

SW3-4 (VGA Routing Control)

This switch controls the routing of VGA signals to either the front or rear of the board. The default switch configuration routes VGA signals to the faceplate video connector.

SW3-4		**Function**
Open	Default	VGA routed to the video connector on the faceplate
Closed		VGA routed to the J5 Rear Panel I/O connector

SW4-1, SW4-2 (Software Configuration)

These switch segments provide configuration information to the user's software. The Switch Monitor register (Port E3h Bits 0-3) monitors the status of SW4 segments as listed below. An open switch reads back a 0; a closed switch reads back a 1. The factory default is open for both switches. The switch segments correspond to register bits as follows:

SW4-1 = Bit 0;   **SW4-2** = Bit 1

See "Switch Monitors (E3h)" in Section 12 for the Switch Monitor Register (E3h) definition.

SW4-3 (Console Redirection)

Console Redirection provides a serial communication link (through COM1) between a terminal or terminal emulation program and the ZT 5515*e*. This feature requires specific parameters to be set in the BIOS Setup utility before configuring SW4-3.

SW4-3		Function
Open	Default	Console redirection *disabled*
Closed		Console redirection *enabled*

Refer to the "Console Redirection" section in the *Performance Technologies Embedded BIOS Manual* before attempting to use this feature.

SW4-4 (BMC Dual Domain Mode)

The BMC on ZT 5515*e* is able to work as a Baseboard Management Controller or Satellite Management Controller by toggling the SW4-4. Normally, the ZT 5515*e* expects there to be a Baseboard Management Controller on the IPMI bus. Close this switch when you do not have a BMC in the chassis.

SW4-4		Function
Open	Default	ZT 5515*e* is a Satellite Management Controller
Closed		ZT 5515*e* is a Baseboard Management Controller

SW5 (Ejector Switch)

The ejector handles are used when ZT 5515*e* is inserted or removed (hot swapped) from a chassis that is powered on. When a customer wishes to remove a board from a system that is powered on, the ejector handles should be opened just enough to disengage the handles from the chassis, but without fully disengaging the bus connectors from the back of the chassis. This triggers a shutdown of the operating system. The BMC then powers off the board and lights the blue hot swap LED on the front panel. Once the blue LED on the front of the board is lit, then it is safe to remove the board from the chassis.

NOTE: In order for the shutdown sequence of the OS to take place a hot swap driver must be installed into the OS. See the ZT 5515*e* support page for this driver or procure the ZT 5515*e* hot swap kit.

The SW5 (ejector handles) need to be closed in order for the board to boot up.

3.3 Jumper Descriptions

J29 (BIOS Configuration Mode)

The ZT 5515*e* includes one 3-pin jumper for the purpose of configuring the BIOS. See Figure 6, "Default Switch Configuration," for its location.

J29		Function
1-2	Default	Normal operation. The BIOS uses its current configuration and password for booting.
2-3		Configuration mode. After POST runs, the system automatically enters the BIOS Setup screen and the maintenance menu is displayed.

Section
4 Connectors

4.1 Overview

As shown in the "Connector Locations" figure, the ZT 5515*e* includes several connectors to interface to application-specific devices. A brief description of each connector is given in the "Connector Assignments" table below. A detailed description and pinout for each connector is given in the following topics.

Table 4. Connector Assignments

Connector	Function
J1	CompactPCI Bus Connector (110-pin, 2 mm x 2 mm, female)
J2	CompactPCI Bus Connector (110-pin, 2 mm x 2 mm, female)
J3	CompactPCI Ethernet Connector (95-pin, 2 mm x 2 mm, female)
J5	Rear-panel I/O Connector (110-pin 2 mm x 2 mm, female)
JA1	Ethernet A Connector (8-pin)
J8	IDE Connector (primary channel – local hard drive)
J11, J12, J14	PCI Mezzanine Connectors (64-pin, 1 mm)
J20	Universal Serial Bus Connector (4-pin, USB, Port 0)
J24	Right Angle DIMM Connector
J25	VGA Connector (15-pin, D-Shell)
J30	COM1 Serial Port (8-pin, RJ-45)

Figure 7. Connector Locations

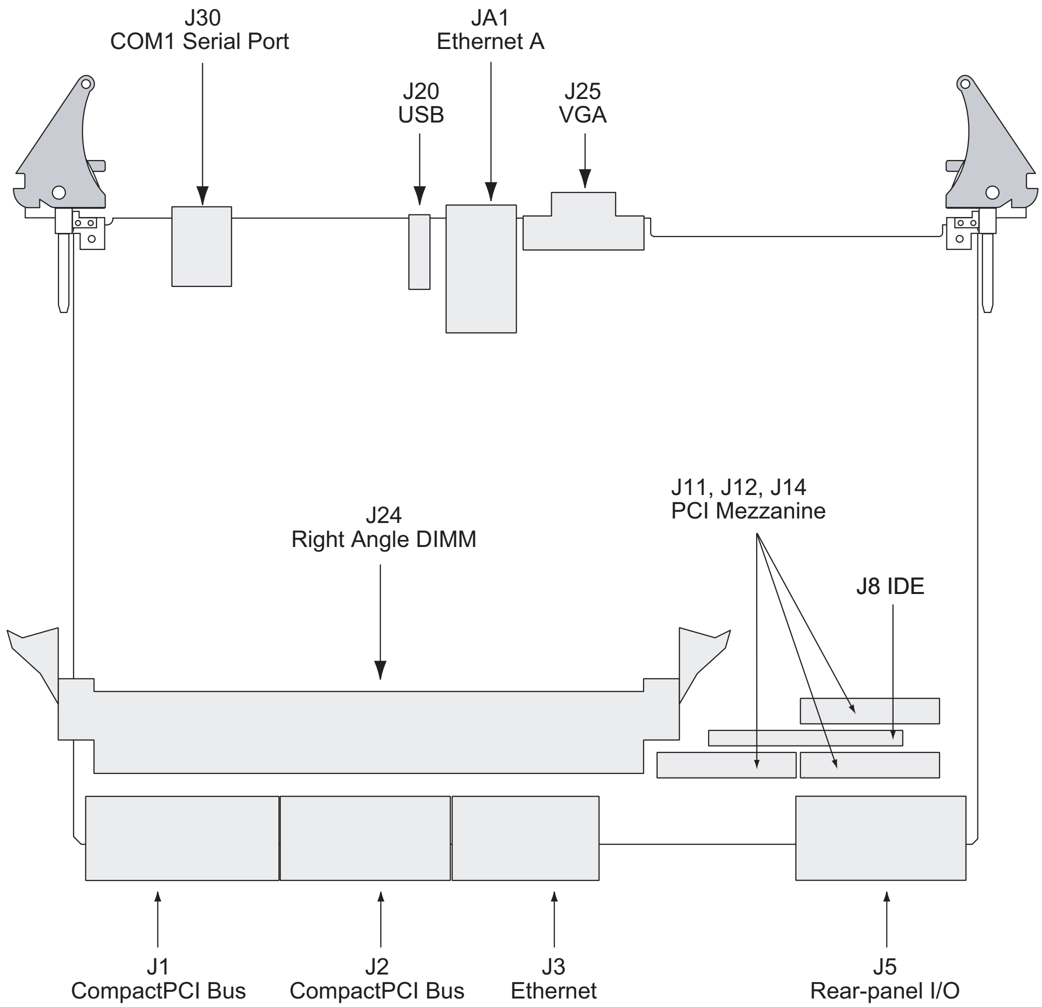
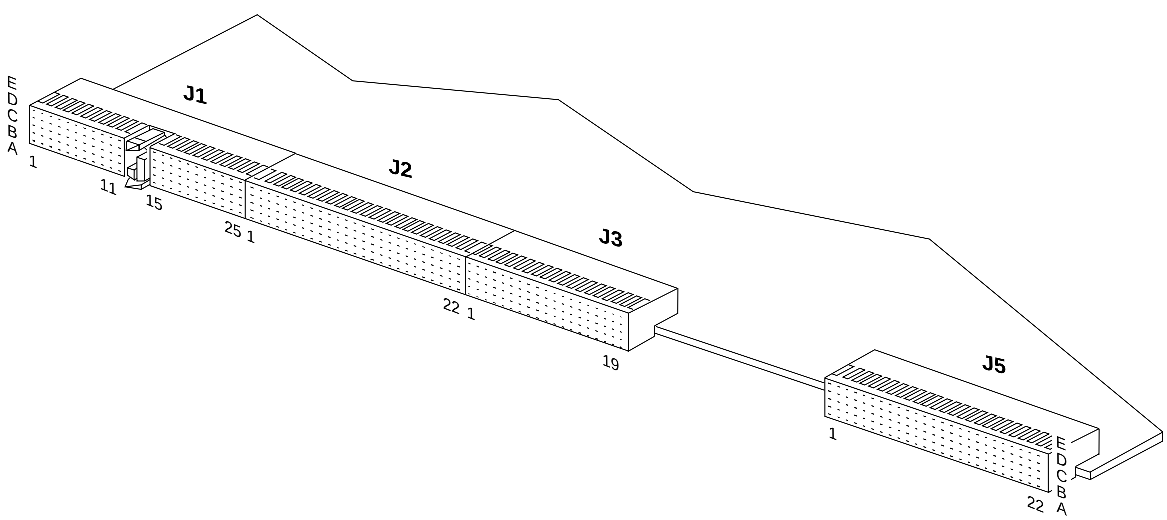


Figure 8. Backplane Connectors - Pin Locations



4.2 Backplane Connectors

J1 (CompactPCI Bus Connector)

J1 is a 110-pin, 2 mm x 2 mm, female 32-bit CompactPCI connector (AMP 352068-1). Rows 12-14 are used for connector keying. See the "J1 CompactPCI Bus Connector Pinout" table below for pin definitions. Refer to the "Backplane Connectors – Pin Locations" illustration for pin placement and the "Connector Locations" illustration for connector identification.

Table 5. J1 CompactPCI Bus Connector Pinout

Pin#	A	B	C	D	E	F
25	5V	REQ64#	ENUM#	3.3V	5V	GROUND SHIELD
24	AD[1]	5V	V(I/O)	AD[0]	ACK64#	
23	3.3V	AD[4]	AD[3]	5V	AD[2]	
22	AD[7]	GND	3.3V	AD[6]	AD[5]	
21	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	
20	AD[12]	GND	V(I/O)	AD[11]	AD[10]	
19	3.3V	AD[15]	AD[14]	GND	AD[13]	
18	SERR#	GND	3.3V	PAR	C/BE[1]#	
17	3.3V	IPMB_CLK	IPMB_DATA	GND	PERR#	
16	DEVSEL#	GND	V(I/O)	STOP#	LOCK	
15	3.3V	FRAME#	IRDY#	BD_SEL#	TRDY#	
KEY						
11	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	
10	AD[21]	GND	3.3V	AD[20]	AD[19]	
9	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	
8	AD[26]	GND	V(I/O)	AD[25]	AD[24]	
7	AD[30]	AD[29]	AD[28]	GND	AD[27]	
6	REQ#	PCI_PRESENT#	3.3V	CLK	AD[31]	
5	BRSVP1A5	BRSVP1B5	PCI_RST#	GND	GNT#	
4	IPMB_PWR	HEALTHY#	V(I/O)	INTP	INTS	
3	INTA#	INTB#	INTC#	5V	INTD#	
2	TCK	5V	TMS	TDO	TDI	
1	5V	-12V	TRST	+12V	5V	

Notes:

(shaded) = Interfaces to long connector pins on the backplane

(bold box) = Interfaces to short connector pins on the backplane

Row F interfaces to long connector pins on the backplane

All other signals interface to medium length connector pins on the backplane

J2 (CompactPCI Bus Connector)

J2 is a 110-pin 2 mm x 2 mm female 64-bit CompactPCI connector (AMP 352152-1). See the "J2 CompactPCI Bus Connector Pinout" table for pin definitions, the "Backplane Connectors - Pin Locations" illustration for pin placement and the “Connector Locations” illustration for connector identification.

Table 6. J2 CompactPCI Bus Connector Pinout

Pin#	A	B	C	D	E	F
22	GA4	GA3	GA2	GA1	GA0	GROUND SHIELD
21	SS_CLK6	SS_GND2	RSVC21	RSVD21	PRTACH	
20	SS_CLK5	SS_GND3	RSVC20	GND	HEART	
19	SS_GND4	SS_GND1	SMBDATA	SMBCLK	SMBALERT-	
18	BRSVP2A18	BRSVP2B18	BRSVP2C18	GND	BRSVP2E18	
17	BRSVP2A17	GND	SS_PRST	SS_REQ6	SS_GNT6	
16	BRSVP2A16	BRSVP2B16	SS_DEG-	GND	BRSVP2E16	
15	J2STAGEEN#	GND	SS_FAL-	SS_REQ5	SS_GNT5	
14	AD[35]	AD[34]	AD[33]	GND	AD[32]	
13	AD[38]	GND	V(I/O)	AD[37]	AD[36]	
12	AD[42]	AD[41]	AD[40]	GND	AD[39]	
11	AD[45]	GND	V(I/O)	AD[44]	AD[43]	
10	AD[49]	AD[48]	AD[47]	GND	AD[46]	
9	AD[52]	GND	V(I/O)	AD[51]	AD[50]	
8	AD[56]	AD[55]	AD[54]	GND	AD[53]	
7	AD[59]	GND	V(I/O)	AD[58]	AD[57]	
6	AD[63]	AD[62]	AD[61]	GND	AD[60]	
5	C/BE[5]#	64EN-	V(I/O)	C/BE[4]#	PAR64	
4	V(I/O)	J2_BPID#	C/BE[7]#	GND	C/BE[6]#	
3	SS_CLK4	GND	SS_GNT3	SS_REQ4	SS_GNT4	
2	SS_CLK2	SS_CLK3	SYSEN-	SS_GNT2	SS_REQ3	
1	SS_CLK1	GND	SS_REQ1	SS_GNT1	SS_REQ2	
Pin#	**A**	**B**	**C**	**D**	**E**	**F**

J3 (CompactPCI Connector)

J3 is a 95-pin 2 mm x 2 mm female connector (AMP 352171-1). See the "J3 Connector Pinout" table below for pin definitions, the "Backplane Connectors - Pin Locations" illustration for pin placement and the “Connector Locations” illustration for connector identification.

Table 7. J3 Connector Pinout

Pin#	A	B	C	D	E	F
19	NC	NC	NC	NC	NC	GROUND SHIELD
18	MDIOAX0+	MDIOAX0-	GND	MDIOAX2+	MDIOAX2-	
17	MDIOAX1+	MDIOAX1-	GND	MDIOAX3+	MDIOAX3-	
16	MDIOBX0+	MDIOBX0-	GND	MDIOBX2+	MDIOBX2-	
15	MDIOBX1+	MDIOBX1-	GND	MDIOBX3+	MDIOBX3-	
14	VCC3	VCC3	VCC3	VCC	VCC	
13	PMC IO [1]	PMC IO [2]	PMC IO [3]	PMC IO [4]	PMC IO [4]	
12	PMC IO [6]	PMC IO [7]	PMC IO [8]	PMC IO [9]	PMC IO [10]	
11	PMC IO [11]	PMC IO [12]	PMC IO [13]	PMC IO [14]	PMC IO [15]	
10	PMC IO [16]	PMC IO [17]	PMC IO [18]	PMC IO [19]	PMC IO [20]	
9	PMC IO [21]	PMC IO [22}	PMC IO [23]	PMC IO [24]	PMC IO [25]	
8	PMC IO [26]	PMC IO [27]	PMC IO [28]	PMC IO [29]	PMC IO [30]	
7	PMC IO [31]	PMC IO [32]	PMC IO [33]	PMC IO [34]	PMC IO [35]	
6	PMC IO [36]	PMC IO [37]	PMC IO [38]	PMC IO [39]	PMC IO [40]	
5	PMC IO [41]	PMC IO [42]	PMC IO [43]	PMC IO [44]	PMC IO [45]	
4	PMC IO [46]	PMC IO [47]	PMC IO [48]	PMC IO [49]	PMC IO [50]	
3	PMC IO [51]	PMC IO [52]	PMC IO [53]	PMC IO [54]	PMC IO [55]	
2	PMC IO [56]	PMC IO [57]	PMC IO [58]	PMC IO [59]	PMC IO [60]	
1	PMC IO [61]	PMC IO [62]	PMC IO [63]	PMC IO [64]	VIO	
Pin#	A	B	C	D	E	F

J5 (Rear Panel I/O CompactPCI Connector)

J5 is a 110-pin 2 mm x 2 mm female connector (AMP 352152-1) providing rear-panel user I/O. See the "J5 Rear Panel I/O Connector Pinout" table below for pin definitions, the "Backplane Connectors - Pin Locations" illustration for pin placement and the "Connector Locations" illustration for connector identification.

Table 8. J5 Rear Panel I/O Connector Pinout

Pin#	A	B	C	D	E	F
22	USB0+	USB0-	SW-5V	USB1+	USB1-	GROUND SHIELD
21	SW-3.3V	GND	GND	GND	GND	
20	RED	GND	H-SYNC	GND	SMBD	
19	GND	SW-5V	GND	SW-5V	SMBC	
18	GREEN	GND	V-SYNC	GND	SMBA-	
17	GND	RSVD	RPIO_PRESENT#	RSVD	IPMB_PWR	
16	BLUE	GND	DDCCLK	KBDAT	KBCLK	
15	GND	SW-5V	DDCDAT	MSDAT	MSCLK	
14	S1RTS	S1CTS	S1R1N	S1DTR	ENETA-LINK	
13	S1DCD	S1TXD	S1RXD	S1DSR	ENETA-ACT	
12	S2RTS	S2CTS	S2RIN	S2DTR	ENETB-LINK	
11	S2DCD	S2TXD	S2RXD	S2DSR	ENETB-ACT	
10	TRK0-	WP-	RDATA-	HDSEL-	DSKCHG-	
9	MTR1-	DIR-	STEP-	WDATA-	WGATE-	
8	DENSL	INDEX-	MTR0-	DR1-	DR0-	
7	CS1S-	CS3S-	DA1	RPELED	RPEJECT-	
6	PWRGD	SPKR	NMI-	DA0	DA2	
5	DDRQ	IORDY	DIOW-	DDACK	DIOR-	
4	DD14	DD0	IDE_ACT	DD15	DRV-IRQ	
3	DD3	DD12	DD2	DD13	DD1	
2	DD9	DD5	DD10	DD4	DD11	
1	PBRST-	DRST-	DD7	DD8	DD6	
Pin#	A	B	C	D	E	F

Legend						
IDE	COM Port	ENET LED	Video	Power	USB	PWRGD
Floppy	Eject	PS/2	SMBus	Ground	Misc	RESV

4.3 Front Panel Connectors

JA1 (Ethernet A Connector)

JA1 (Ethernet A) is an 8-pin RJ-45 connector providing 10 Mb (10BASE-T), 100 Mb (100BASETX) and 1000 Mb (1000BASE-TX) protocols out the front of the board. Two LEDs are located inside each RJ-45 connector:

First LED:

- Green indicates a link
- Blinking Green indicates activity

Second LED:

- Off = 10 MB
- Green = 100 MB
- Yellow = 1000 MB

See the “JA1 Ethernet A Connector Pinout” table below for pin definitions and the “Connector Locations” illustration for connector identification.

Ethernet A signals can either be directed out the front JA1 port or out J3 to the backplane. Whether Ethernet A is routed out the front or the rear is an option in the system BIOS. Enter the BIOS Setup screen by pressing “F2” while the system is boot through POST. See “BIOS Configuration Overview“ in Section 2 for more information.

Table 9. JA1 Ethernet A Connector Pinout

Pin#	Function
1	TRCT3
2	TRD3-
3	TRD3+
4	TRD2+
5	TRD2-
6	TRCT2
7	TRCT4
8	TRD4+
9	TRD4-
10	TRD1-
11	TRD1+
12	TRD1+

J25 (VGA Connector)

J25 is a 15-pin, female, D-shell connector (AMP 748390-9) providing a front panel interface for VGA signals. See the "J25 VGA Connector Pinout" table for pin definitions and the “Connector Locations” illustration for connector identification.

Video signals can also be directed out J5 to an RTM. See switch SW3-4.

Table 10. J25 VGA Connector Pinout

Pin#	Signal
1	RED
2	GREEN
3	BLUE
4	NC
5	DGND

Pin#	Signal
6	RGND
7	GGND
8	BGND
9	+5V (fused)
10	SGND

Pin#	Signal
11	NC
12	DDC DAT
13	HSYNC
14	VSYNC
15	DDC CLK

J20 (Universal Serial Bus 0 Connector)

J20 (Port0) is a Universal Serial Bus (USB) Interface connector (AMP 440260-1). See the “J20 Universal Serial Bus 0 Connector Pinout” table below for pin definitions and the “Connector Locations” illustration for connector identification.

USB port 0 is available only from the front USB connector but USB Ports 2 and 3 are routed out J5 for use with an RTM.

Table 11. J20 Universal Serial Bus 0 Connector Pinout

Pin#	Function
1	Vcc (Fused)
2	DATA-
3	DATA+
4	GND

J30 (COM1 Serial Port)

J30 is an RJ-45 connector providing a front-panel COM1 interface. COM1 signals are also directed out J5 to the backplane. See the "J30 COM1 Serial Port Pinout" table below for pin definitions and the “Connector Locations” illustration for connector identification. SRI (Serial Ring Indicator) and SCD (Serial Carrier Detect) signals are not included in the front panel RJ-45 connector.

NOTE: COM1 signals are available to the front and rear panel (at J5) simultaneously. Utilizing COM1 at the front and rear at the same time will cause a signaling conflict.

Table 12. J30 COM1 Serial Port Pinout

Pin#	Function	Pin#	Function
1	RTS	6	RXD
2	DTR	7	DSR
3	TXD	8	CTS
4	GND	-	SRI
5	GND	-	SCD

4.4 Internal Connectors

J11, J12 and J14 (PCI Mezzanine Connectors)

J11, J12 and J14 are 64-pin, 1.00mm, dual row, vertical stacking receptacles providing a PCI local bus interface to optional PMC cards. These connectors provide a complete 32-bit PCI interface. See the following "J11 PCI Mezzanine Connector Pinout," J12 PCI Mezzanine Connector Pinout" and "J14 PCI Mezzanine Connector Pinout" tables for pin definitions and the “Connector Locations” illustration for connector identification.

Table 13. J11 PCI Mezzanine Connector Pinout

Pin	Signal
1	NC
3	GND
5	B0_INTD-
7	NC
9	B0_INTB-
11	GND
13	PMCB_PCICLK
15	GND
17	PMC2_REQ-
19	VIO (VCC3)
21	B0_PAD28
23	B0_PAD25
25	GND
27	B0_PAD22
29	B0_PAD19
31	VIO (VCC3)
33	B0_FRAME-
35	GND
37	B0_DEVSEL-
39	GND
41	NC
43	B0_PAR
45	VIO (VCC3)
47	B0_PAD12
49	B0_PAD9
51	GND
53	B0_PAD6
55	B0_PAD4
57	VIO (VCC3)
59	B0_PAD2
61	B0_PAD0
63	GND

Pin	Signal
2	-12V
4	B0_INTC-
6	B0_INTA-
8	VCC
10	NC
12	NC
14	GND
16	PMC2_GNT-
18	VCC
20	B0_PAD31
22	B0_PAD27
24	GND
26	B0_CBE-3
28	B0_PAD21
30	VCC
32	B0_PAD17
34	GND
36	B0_IRDY-
38	VCC
40	B0_LOCK-
42	NC
44	GND
46	B0_PAD15
48	B0_PAD11
50	VCC
52	B0_CBE-0
54	B0_PAD5
56	GND
58	B0_PAD3
60	B0_PAD1
62	VCC
64	REQ64B

Table 14. J12 PCI Mezzanine Connector Pinout

Pin	Signal	Pin	Signal
1	+12V	2	NC
3	NC	4	NC
5	NC	6	GND
7	GND	8	NC
9	NC	10	NC
11	PMC2-BUSMODE2[1]	12	VCC3
13	B0_PCIRST-	14	PMC2-BUSMODE3[2]
15	VCC3	16	PMC2-BUSMODE4[3]
17	NC	18	GND
19	B0_PAD30	20	B0_PAD29
21	GND	22	B0_PAD26
23	B0_PAD24	24	VCC3
25	PMC2_IDSEL[4]	26	B0_PAD23
27	VCC3	28	B0_PAD20
29	B0_PAD18	30	GND
31	BO PAD16	32	B0_CBE-2
33	GND	34	NC
35	B0_TRDY-	36	VCC3
37	GND	38	B0_STOP-
39	B0_PERR-	40	GND
41	VCC3	42	B0_SERR-
43	B0_CBE-1	44	GND
45	B0_PAD14	46	B0_PAD13
47	GND	48	B0_PAD10
49	B0_PAD8	50	VCC3
51	B0_PAD7	52	NC
53	VCC3	54	NC
55	NC	56	GND
57	NC	58	NC
59	GND	60	NC
61	ACK64B	62	VCC3
63	GND	64	NC

NOTES:

1. PMC2-BUSMODE2 has a 10k pullup to VCC3
2. PMC2-BUSMODE3 has a 10k pulldown to GND
3. PMC2-BUSMODE4 has a 10k pulldown to GND
4. PMC2_IDSEL is connected to B0_PAD31 (PCI device 14h)

Table 15. J14 PCI Mezzanine Connector Pinout

Pin	Signal	Pin	Signal
1	User I/O	2	User I/O
3	User I/O	4	User I/O
5	User I/O	6	User I/O
7	User I/O	8	User I/O
9	User I/O	10	User I/O
11	User I/O	12	User I/O
13	User I/O	14	User I/O
15	User I/O	16	User I/O
17	User I/O	18	User I/O
19	User I/O	20	User I/O
21	User I/O	22	User I/O
23	User I/O	24	User I/O
25	User I/O	26	User I/O
27	User I/O	28	User I/O
29	User I/O	30	User I/O
31	User I/O	32	User I/O
33	User I/O	34	User I/O
35	User I/O	36	User I/O
37	User I/O	38	User I/O
39	User I/O	40	User I/O
41	User I/O	42	User I/O
43	User I/O	44	User I/O
45	User I/O	46	User I/O
47	User I/O	48	User I/O
49	User I/O	50	User I/O
51	User I/O	52	User I/O
53	User I/O	54	User I/O
55	User I/O	56	User I/O
57	User I/O	58	User I/O
59	User I/O	60	User I/O
61	ACK64B	62	User I/O
63	GND	64	User I/O

J8 (IDE Connector)

J8 is a 44-pin, male, 2mm (.079") header (Comm Con Connectors, Inc. 51206), providing a primary IDE channel interface. See the "J14 IDE Connector Pinout" table below for pin definitions and the “Connector Locations” illustration for connector identification.

Table 16. J8 IDE Connector Pinout

Pin#	Signal	Pin#	Signal
1	RST-	2	GND
3	DDP7	4	DDP8
5	DDP6	6	DDP9
7	DDP5	8	DDP10
9	DDP4	10	DDP11
11	DDP3	12	DDP12
13	DDP2	14	DDP13
15	DDP1	16	DDP14
17	DDP0	18	DDP15
19	GND	20	NC
21	PDREQ-	22	GND
23	PDIOW-	24	GND
25	PDIOR-	26	GND
27	PDIORDY	28	CSEL1[1]
29	PDACK-	30	GND
31	IRQ14	32	IOCS16-[2]
33	DAP1	34	PDIAG
35	DAP0	36	DAP2
37	CS1P-	38	CS3P-
39	PDASP	40	CS3P-
41	VCC	42	VCC
43	GND	44	NC

NOTES:

1. CSEL1 has 475Ω pulldown to GND
2. IOCS16- has 10k pullup to VCC3 (+3.3V)

Section

5 Reset

This section discusses the reset types and reset sources on the ZT 5515*e*. If necessary, the ZT 5515*e*'s board reset characteristics can be tailored to the requirements of a specific system.

5.1 Reset Types and Sources

The ZT 5515*e*'s reset types are listed below. The sources for each reset type are detailed in the following topics.

- **Hard Reset:** All devices are held in reset.
- **Soft Reset:** CPU initialization only. Other devices are not reset.
- **Backend Power Down:** The backend logic is powered off. The board is powered on and is held in reset.
- **NMI:** Non-maskable interrupt. Though not a reset in the strict sense, an NMI can have the same effect as other resets.

Hard Reset Sources

System Register CF9h (ICH4 Reset Control Register)

Bits 1 and 2 in this register are used by the ICH4 to generate a hard reset or a soft reset. During a hard reset, the ICH4 asserts CPURST, PCIRST#, and RSTDRV. Additionally, it resets its core and suspend well logic.

Soft Reset Sources

System Register CF9h (ICH4 Reset Control Register)

Bits 1 and 2 in this register are used by the ICH4 to generate a hard reset or a soft reset. During a soft reset, the ICH4 asserts INIT to the CPU for 16 PCICLK. This causes the processor to enter "real mode," initialize its internal registers, and begin instruction execution from FFFFFFF0h (the boot vector).

Keyboard Controller Reset

The keyboard controller generates a keyboard controller reset when FEh is written to port 64h. This causes the ICH4 to assert INIT to the CPU.

Keyboard CTRL-ALT-DEL

Simultaneously pressing these keys calls a BIOS function that reboots the system.

NOTE: This method does not work under operating systems that trap calls to this BIOS function.

Watchdog Timer (System Register Address 79h)

The watchdog timer may be programmed to generate a "CPU Init" if it is not strobed within a given time-out period. This function is discussed in Section 7, "Watchdog Timer."

Backend Power Down Sources

Board Extraction

When a board is extracted from an enclosure (specifically, when the "board-select" [BD-SEL] pin is disengaged), the hot swap controller unconditionally removes backend power from the board and holds the board in reset.

Low Voltage

When any of the 3.3V, 5V, or 12V supply voltages are detected to be below an acceptable operating limit, the hot swap controller unconditionally removes backend power and holds the board in reset.

Overcurrent Fault

If a power fault condition (overcurrent) is detected, the hot swap controller removes backend power and turns the Health LED red. The board is held in reset.

NMI Sources

Watchdog Timer (System Register Address 79h)

The watchdog timer may be programmed to generate a non-maskable interrupt if it is not strobed within a given time-out period. This function is discussed in Section 8, "Watchdog Timer."

Section

6

System Monitoring and Control

The ZT 5515*e* performs system control and monitoring functions using an Intel Baseboard Management Controller (BMC) ASIC, the VT22030A. The BMC has the following features:

- IPMB_PWR delivers 5VDC (1A/pin) to the BMC; other required voltages are derived from this power source.
- Power ramping controls inrush current and avoids glitching the IPMB power rail.
- On power-up, the BMC is held in reset until power is stable.
- A 1024K x 8 flash device and a 32K x 8 SRAM device are used for code and data storage.
- Six IPMI-compliant Interfaces are available.

In the event that IPMB Power is not available, the BMC draws power from BP_VCC to allow backward compatibility. The BMC and all its local monitoring devices are powered from the IPMB Power source allowing the BMC to monitor and control the local CPU without backplane or local power.

6.1 Monitoring and Control Functions

The BMC tracks the heartbeat of the host CPU by monitoring several parameters on the ZT 5515*e*. Most of these parameters are measured by the Analog Devices, ADM1026, System Monitoring Device. Monitoring and control functions are listed below.

Monitoring Functions

- Onboard Power Supplies, +3.3V, +5V, +12V, and –12V supplies
- Chipset and memory power supplies : +2.5V, +1.25V, +1.8V, +1.5V
- CPU Core Supply
- Onboard and CPU Temperatures
- CPU VID Lines
- Eject signals from front- and rear-panel
- Global Addressing Bits GA[0:4]
- SIO Low Frequency Clock (Real Time Clock Monitoring Frequency from SIO)
- Power OK
- Hot swap controller fault condition
- Back end Power Fail and Power Degrade signals
- SMBUS Alert signals
- PCI_PRESENT#, SYSSLOT#, BDSEL# for dual domain mode support

Control Functions

- CPU board Reset Control
- CPU board power on/power off control
- CPU NMI Assertion to processor
- Dual Domain Mode

Field Replaceable Unit (FRU) Information

The BMC controller stores the FRU information about the board and RTM. Each device has its own address. This device is a 32K x 8 device used to hold information about the card.

Host CPU controller = Device 0

Host CPU RTM = Device 1

System Event Log Information

The BMC controller stores system event information in an 8K x 8 serial EEPROM device. Both the in-band KCS interface and the out-of-band IPMB interface provide access to the System Event Log (SEL). This allows SEL information to be accessed through the IPMB interface even if the system is down.

6.2 SMBus Address Map

The table below lists the location, function, and address of each SMBus device used on the ZT 5515*e*.

Table 17. SMBus Device Details

Device	ZT 5515*e* Function	Address
ADM1026	CPU voltage and temperature monitoring	0101100
Ethernet A	Ethernet controller A	0001000
Ethernet B	Ethernet controller B	0001001
FRU	Field Replaceable Unit SEEPROM	1010011
SEL	System Event Log SEEPROM	1010011
DDR SDRAM	Signal Presence Detect (SPD) PROM	1010000
CK408	Clock generator	1101001

Section

7 IDE Controller

The ZT 5515*e*A-1B has an on-board IDE controller that provides two IDE channels for interfacing with up to four IDE devices. The IDE controller is incorporated into the Intel 845E chipset which supports ATA-100. There is one 44-pin IDE connector on the ZT 5515*e*A-1B, which supports up to two IDE devices (though there is only space on the board itself to mount one device). The secondary IDE channel is available through the rear panel connector (J5).

"Intel 845E Chipset" in Section 13 provides a link to the PIIX4E datasheet.

7.1 Features of the IDE Controller

- Primary and secondary channels for interfacing up to four devices
- IBM-AT compatible
- Supports PIO and Bus Master IDE
- "Ultra ATA/33/66/100" synchronous DMA operation
- Bus Master IDE transfers up to 100 MB/sec.
- Individual software control for each IDE channel
- 32-bit, 33 MHz, high performance PCI bus interface

7.2 Disk Drive Support

The ZT 5515*e* supports internal and external IDE devices. These configurations are described below.

7.3 Primary IDE Channel

The ZT 5515*e*'s primary IDE channel is directed to the J8 IDE connector. J8 is used to interface with the locally mounted hard drive. For specifications of the J8 IDE connector, see "J30 (COM1 Serial Port)" in Section 4.

7.4 Secondary IDE Channel

The ZT 5515*e*'s secondary IDE channel is directed via the J5 rear-panel I/O connector to a compatible RTM, such as the ZT 4807*e*. See "J5 (Rear Panel I/O CompactPCI Connector)" in Section 4 for specifications of the J5 connector.

Refer to the *ZT 4807e Packet Switched Rear Panel Transition Board Hardware Manual* for product information.

7.5 IDE I/O Mapping

The I/O map for the IDE interface varies depending on the mode of operation. The default mode is “compatibility mode,” meaning that the interface uses the PC-AT legacy addresses of 1F0h-1F7h, with 3F6h and interrupt IRQ14 for the primary channel. The secondary channel uses I/O addresses 170h-177h, 376h and interrupt IRQ15. No memory addresses are used.

7.6 IDE CompactFlash Carrier

Performance Technologies provides an optional IDE CompactFlash Carrier (ZT 96080) that can be mounted in the hard drive location on the ZT 5515*e*A-1B (the ZT 5515*e*A-1A does not support this CompactFlash carrier on the main board because it does not have an IDE connector). This carrier accommodates multiple types of CompactFlash cards, which appear to the system as a hard drive, and are automatically supported by most operating systems. For more information about the ZT 96080 CompactFlash Carrier, see the Performance Technologies Web site.

7.7 IDE Device Drivers

The IDE interface works with all applications by default. To fully utilize the IDE interface, additional software drivers may need to be installed. Contact the vendor of your intended operating system to receive the latest drivers.

Section 8 Watchdog Timer

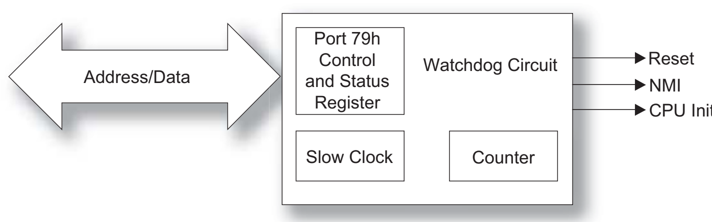
This section explains the operation of the ZT 5515*e*'s watchdog timer. It provides an overview of watchdog operation and features, as well as sample code to help you learn how the watchdog timer works with applications.

8.1 Watchdog Timer Overview

The primary function of the watchdog timer is to monitor the ZT 5515*e*'s operation and take corrective action if the software fails to function as programmed. The major features of the watchdog timer are:

- Two-stage operation (meaning that it can be enabled to produce a non-maskable interrupt [NMI] or a "CPU init" before it generates a reset)
- Enabled and disabled through software control
- Armed and strobed through software control

Figure 9. Watchdog Timer Architecture



The ZT 5515*e*'s custom watchdog timer circuit is implemented in a programmable logic device. The watchdog timer contains a control and status register that is documented in Section 11 as Watchdog (79h). The register allows applications to determine if a watchdog timeout caused a particular reset.

The watchdog timer drives the first and second stages as follows:

1. The watchdog times out (first stage) after a selected timeout interval.
2. NMI or INIT (software selectable) is driven high.
3. A hard reset occurs (second stage) 250 ms later.

Eight timeout intervals are selectable through bits 0-2 of the register. The intervals range from a minimum of 250 ms to a maximum of 256 seconds. See Watchdog (79h) in Section 12 for all possible timeout periods. A register bit can be enabled to indicate if the watchdog timer caused the reset event. The watchdog timer register is cleared on power-up, enabling the system software to take appropriate action if the watchdog generated the reboot.

The watchdog is normally strobed by reading the watchdog register (79h), which clears the counter. Writes to this register also clear the counter.

Power Up Initialization

The watchdog timer's logic is initialized at power up. This ensures that the stage1 monitor, stage2 monitor, stage1 enable, and stage2 enable status and control bits power up to unasserted states (0). This allows an application to determine if the reset was caused by a watchdog timeout or a power up.

Timeout Values

The watchdog timer has a separate slow clock source that runs at a maximum frequency of 32 Hz (25 Hz nominal). Because the clock is based on an RC oscillator, the nominal timeout period is approximately 30% longer than the minimum value. The watchdog is guaranteed to timeout in no less than the programmed minimum value.

Using the Watchdog in an Application

The following topics are provided to aid you in learning to use the watchdog in an application. The watchdog's reset and NMI functions are described and sample code is provided.

Watchdog reset and NMI are controlled through the watchdog control and status register, documented in Section 12 as Watchdog (79h).

Watchdog Reset

An application using the reset feature enables the watchdog reset, sets the terminal count period, and then periodically strobes the watchdog to keep it from resetting the system. If a strobe is missed, the watchdog times out and resets the system hardware.

Enabling the Watchdog Reset

C code for enabling the watchdog reset might look like the following:

```
#define WD_RESET_EN_BIT_SET_0x20

void EnableWatchdogReset(void){
unsigned char WdValue;            // Holds watchdog register values.
                                  //
WdValue = inb(WD_CSR_IO_ADDRESS);// Read the current contents of the
                                  // watchdog register.
WdValue |= WD_RESET_EN_BIT_SET;   // Assert the enable bit in the
                                  // local copy.
outb(WD_CSR_IO_ADDRESS,WdValue);  // Assert the enable in the
                                  // watchdog register.
}
```

Setting the Terminal Count

The terminal count determines how long the watchdog waits for a strobe before resetting the hardware. C code for setting the terminal count might look like the following:

```
#define WD_CSR_IO_ADDRESS  0x79   // IO address of the watchdog
#define WD_T_COUNT_MASK    0x07   // Bit mask for terminal count bits.
#define WD_500MS_T_COUNT   0x01   // Terminal count values . . . .
#define WD_1S_T_COUNT      0x00   //
#define WD_250MS_T_COUNT   0x00   //
.
.
.
void SetTerminalCount(void){
unsigned char WdValue;            // Holds watchdog register values.
                                  //
WdValue = inb(WD_CSR_IO_ADDRESS);// Get the current contents of the
                                  // watchdog register.
WdValue &= ~ WD_T_COUNT_MASK;     // Mask out the terminal count bits.
WdValue |= WD_500MS_T_COUNT;      // Set the desired terminal count.
outb(WD_CSR_IO_ADDRESS,WdValue); // Furnish the watchdog register
                                  // with the new count value.
}
```

Strobing the Watchdog

Once the watchdog is enabled, it must be periodically strobed within the terminal count period to avoid resetting the system hardware. C code to strobe the watchdog might look like the following:

```
void StrobeWatchdog(void){
inb(WD_CSR_IO_ADDRESS);    // A single read is all it takes.
}
```

Watchdog NMI

When enabled, an NMI precedes a watchdog reset by 250 ms. The NMI generation feature gives an application 250 ms to perform essential tasks before the hardware is reset. Before using watchdog NMI, ensure the following:

- The essential task code is included in an interrupt service routine (ISR).
- The ISR is chained to the existing NMI ISR.
- The watchdog NMI is enabled.

Chaining the ISRs

Save the original NMI ISR vector so that it can be invoked from the new watchdog NMI ISR. Alter the interrupt vector table so that the NMI ISR vector is overwritten with a vector to the watchdog ISR. C code to do this in DOS might look like the following:

```
#define NMI_INTERRUPT_VECTOR_NUMBER 2

void interrupt far (*OldNmiIsr)();

void HookWatchdogIsr(void){
```

```
//
// To be absolutely certain the interrupt table is not accessed by an
// NMI (this is quite unlikely), the application could disable NMI in
// the chip set before installing the new vector.
//
.
.
.
//
// Install the new ISR.
//
oldNmiIsr = getvect(IsrVector);                // Save the old vector.
setvect(NMI_INTERRUPT_VECTOR_NUMBER, WatchdogIsr);   // Install the new.
}
```

Enabling the Watchdog NMI

To activate the NMI feature, enable it in the watchdog register (Port 79h). The code to do this might look like the following:

```
#define WD_NMI_EN_BIT_SET  0x10
void EnableWatchdogNmi(void){
unsigned char WdValue;           // Holds watchdog register values.
                                 //
WdValue = inb(WD_CSR_IO_ADDRESS);// Read the current contents of the
                                 // watchdog register.
WdValue |= WD_NMI_EN_BIT_SET;    // Assert the enable bit in the
                                 // local copy.
outb(WD_CSR_IO_ADDRESS,WdValue); // Assert the enable in the watchdog
                                 // register.
}
```

NMI Handler

Because an NMI may originate from a source such as a RAM Error Correction Code (ECC) error, the NMI handler cannot assume that an NMI occurred due to a watchdog timeout. Therefore, the NMI handler must check the watchdog status register before taking watchdog-related emergency action. When the NMI handler completes handling the emergency, it invokes the original NMI Handler (discussed above). The code to do this might look like the following:

```
#define WD_NMI_DETECT_BIT_SET     0x40   // Bit indicates an NMI occurred,
                                         // set.
                                         //
void WatchdogIsr(void){                  //
                                         //
                                         //
                                         // Did the watchdog cause the
                                         // NMI?
                                         //
if(inb(WD_CSR_IO_ADDRESS) & WD_NMI_DETECT_BIT_SET){
                                         //
             TripAlarm();                // Take care of essential tasks.
                                         //
             TurnOffTheGas();            //
       }                                 //
       _chain_intr(OldNmiIsr);           // Invoke the originally
                                         // installed ISR.
}
```

Section
9 System BIOS

The embedded BIOS on the ZT 5515*e* is implemented as firmware that resides in the on-board flash read-only memory (ROM). The BIOS contains standard PC-compatible basic input/output (I/O) services and standard server features.

Support for applicable SBC peripheral devices (SCSI, NIC, video adapters, etc.), that are also loaded into the SBC flash ROM, are not specified in this document. Hooks are provided to support adding BIOS code for these adapters; the binaries must be obtained from the peripheral device manufacturers and loaded into the appropriate locations.

9.1 On-Board Flash Memory

The ZT 5515*e* provides 16 MB of on-board flash memory. The first 1 MB of this memory is used to hold the system BIOS, and an additional 1 MB stores the secondary system BIOS. The remaining 14 MB are for customer use and can be used to store an operating system such as VxWorks.

To reprogram the BIOS or update it if it becomes corrupted, use the BIOS recovery module and flash.exe utility available from Performance Technologies and discussed later in this section.

The flash memory is write-protected through switch SW2-1. See "SW2-1 (Flash Write-Protect)" in Section 3 for more information.

Flash Utility Program

Flash.exe is a utility program that is available on the Performance Technologies Web site. Run flash.exe to modify the BIOS in the on-board flash memory. flash.exe eliminates the need for a PROM programmer and for removing boards and chips from the system.

Before attempting to program the flash, make sure that switch SW2-1 is open (see "SW2-1 (Flash Write-Protect)" in Section 3).

To reprogram the BIOS on the ZT 5515*e*:

1. Download the latest BIOS for the ZT 5515*e* from the Performance Technologies Web site. Normally, the BIOS zip file also contains the flash.exe utility you need.
2. Create a DOS 6.2 boot disk and add the BIOS file and flash utility to the disk. Usually other Windows boot disks work fine as well, but use DOS if you run into any problems.
3. Boot the ZT 5515*e* from the DOS boot disk you just created. You can do this via either a USB Floppy or off a ZT 4807*e* RTM. The ZT 4807*e* provides a standard floppy connector. If your system does not boot off the floppy drive, you may need to enter the BIOS setup in order to move the floppy to the first item in the boot order.
4. Use the following syntax at a DOS prompt:

FLASH /b BIOS.XXX

where BIOS.XXX is the BIOS image for the ZT 5515*e*.

See the *Performance Technologies Embedded BIOS Manual* for more information on the flash utility. The BIOS zip file should also contain a Readme file or installation file to help guide you through BIOS installation.

9.2 BIOS Configuration Overview

This topic presents a brief introduction to the Performance Technologies Embedded BIOS. For more detailed information about the BIOS and other utilities, see the *Performance Technologies Embedded BIOS (AMI Core) Software Manual*.

The Performance Technologies Embedded BIOS has many separately configurable features. These features are selected by running the built-in Setup utility. The system configuration settings are saved in a portion of the battery-backed RAM in the real-time clock device and are used by the BIOS to initialize the system at boot-up or reset. The configuration is protected by a checksum word for system integrity.

To access the Setup utility, press the **F2** key during POST test and initialization at boot time. Setup runs once the POST functions complete.

When Setup runs, an interactive configuration screen displays. Setup parameters are divided into different categories. The available categories are listed in a menu across the top of the Setup screen. The parameters within the highlighted (current) category are listed in the main (left) portion of the Setup screen. Context-sensitive help is displayed in the right portion of the screen for each parameter. A legend of keys is listed at the bottom of the Setup screen.

Use the left and right arrow keys to select a category from the menu. Use the up and down arrow keys to select a parameter in the main portion of the screen. Use the + or – keys to change the value of a parameter.

Items in the main portion of the screen that have a triangular mark to their left are submenus. To display a submenu, use the up and down arrow keys to highlight the submenu and then press the **Enter** key.

9.3 System Information Structure

The System Information Structure (SIS) contains platform-specific information, primarily relating to the type, location, and configuration of the BIOS and flash memory. The table and its information are available to both BIOS routines and user applications.

Implementation

The ZT 5515*e* uses a 16 MB StrataFlash device with no BootBlock, organized into 1 MB pages at FFF00000-FFFFFFFFh using Paging Mechanism 2. The structure was updated to version 1.02 in the latest release.

The SIS table consists of both static information provided at BIOS build time, and dynamic information that is modified when the structure is loaded into shadow RAM during BIOS POST. The dynamic or “running” version of the table is located in the BIOS shadow area near the top of the 1 MB address space. The static version of the table can be extracted from the BIOS image itself, either in flash or from a file on disk.

The elements of the structure that are dynamic depends on the particular platform. For example, a board that is always loaded with the same type and size of flash device could define the `FlashSize` and `FlashID` fields statically, while a product with several flash options would need to be able to modify those fields during POST.

The System Information Structure is defined as follows in C language syntax:

```
typedef struct
{
        UINT8 Signature[8];
        UINT32 SysFlag; /* <-- new flags added Ver 1.02 */
        UINT32 BiosAddr;
        UINT32 BiosNvAddr;
        UINT32 FlashAddr;
        UINT16 CPUtype;
        UINT16 BiosSize;
        UINT16 BiosNvSize;
        UINT16 BiosVersion;
        UINT16 FlashID;
        UINT16 FlashPageSize;
        UINT16 FlashEraseSize;
        UINT16 FDriveSize;
        UINT16 StructureSize;
        UINT16 StructureVersion;
        UINT8 CPUstr[16];
        UINT8 NetworkID[6];
        UINT8 BiosPage;
        UINT8 BiosNvPage;
        UINT8 FlashSize;
        UINT8 FlashCount;
        UINT8 Algorithm;
        UINT8 Mechanism;
        UINT8 FDriveLetter;
        UINT8 ChecksumPad;
        UINT8 NetworkIDPad;
        UINT8 BootBlockPage; /* <-- Ver 1.01 starts here */
        UINT32 BootBlockAddr;
        UINT32 FDriveAddr;
        UINT16 BootBlockSize;
        UINT16 TotalBiosSize;
        UINT8 FDrivePage;
} ZiaSysInfo;
```

Detailed Structure Element Descriptions

Table 18. Detailed Structure Element Descriptions

Name	Offset	Description	Ver
Signature	0	Structure signature. Always = “ZIA INFO”. No terminating zero.	1.00
SysFlag	8	System flags. See Note 1 below.	1.00
BiosAddr	12	32-bit physical address where BIOS starts in flash. See Note 9.	1.00
BiosNvAddr	16	32-bit physical address where BIOS NVRAM starts in flash. See Note 9.	1.00
FlashAddr	20	32-bit physical address where flash memory starts. See Note 9.	1.00
CPUtype	24	Board number in BCD. Ex: 0x5540 for ZT 5540	1.00
BiosSize	26	BIOS Size in KB.	1.00
BiosNvSize	28	BIOS NVRAM Size in KB.	1.00
BiosVersion	30	BIOS Version in BCD. Ex: 0x0115 for version 1.15.	1.00
FlashID	32	Flash memory’s Jedec number.	1.00
FlashPageSize	34	Flash page size in KB, if flash is paged.	1.00
FlashEraseSize	36	Flash block erase size in KB.	1.00
FdriveSize	38	Flash drive size in KB	1.00
StructureSize	40	Size of this table structure in bytes.	1.00
StructureVersion	42	Structure Version in BCD. Ex:0x0115 for 1.15. See Note 6	1.00
CPUstr	44	A 16-byte ASCII string, not zero terminated.	1.00
NetworkID	60	Compactnet Network ID. See Note 2.	1.00
BiosPage	66	BIOS page number, if flash is paged. See Note 3.	1.00
BiosNvPage	67	BIOS NVRAM page number, if flash is paged. See Note 3.	1.00
FlashSize	68	Flash device size in MB.	1.00
FlashCount	69	Number of flash devices.	1.00
Algorithm	70	Flash algorithm. See Note 4 below.	1.00
Mechanism	71	Flash paging and write-protection mechanism. See Note 5.	1.00
FdriveLetter	72	Flash drive letter, 0=A, 1=B, etc.	1.00
ChecksumPad	73	Checksum padding, See Note 7.	1.00

NetworkIDPad	74	BIOS Network ID Padding. See Note 8.	1.00
BootBlockPage	75	BootBlock page number, if flash is paged. See Note 3.	1.01
BootBlockAddr	76	32-bit physical address where BootBlock starts in flash. See Note 9.	1.01
FDriveAddr	80	32-bit physical address of first block of flash drive. See Notes 9 and 10.	1.01
BootBlockSize	84	BootBlock Size in KB.	1.01
TotalBiosSize	86	Total BIOS Size in KB, including BIOS, NVRAM, BootBlock, and any future modules that may be added.	1.01
FDrivePage	88	Page number of first block of flash drive, if flash is paged. See Notes 3 and 10.	1.01

NOTES:

1. These flags are defined. All unused bits are reserved.
   Bit 0: 1 = STD Product
   Bit 1: 1 = CPCI Product
   Bit 2: 1 = CPCI CompactNET System
   Bit 3: 1 = Current Table is contained in a BootBlock(A BIOS with a BootBlock may have 2 tables – one in the BootBlock with this bit set, and another in the main BIOS image with this bit cleared.)
   Bit 4: 1 = AMI BIOS (added ver. 1.02)
2. The 6 byte BIOS network ID is for Compactnet multiprocessing, NOT for the on-board Ethernet.
3. This is page number only, NOT the output value for the I/O port. See Note 5 on how to select a page.
4. The algorithm is defined as follows. All unused bits are reserved.
   1 = Intel flash
   2 = AMD® flash
   3 = Sharp® flash
   4 = Atmel® flash
   5 = Intel Firmware Hub (FWH) flash (added ver. 1.01)
   6 = Intel StrataFlash™ (added ver. 1.01)
5. It is important to remember that the actual method used for write protecting the flash varies, not only between paging mechanisms, but between different boards with the *same* paging mechanism. Write protection may consist of asserting the write protect signal to the flash device, disabling the programming voltage, or simply disabling all write cycles to the device. Because of this, write protection may or may not disable "read-only" flash commands such as Identify. Block locking should be enabled for those flash devices that support it.
   For all current mechanisms, the flash drive grows downward below the BIOS and other related areas. If an OS image is programmed, it starts from the bottom of the flash and grows upward. The mechanisms are defined as follows:
   Mechanism 1:
   Flash is paged. The majority of the BIOS resides at the top of the flash, in page 15 (0x0f) of flash device 0, although it may extend down into other pages. This top page is selected by port 0x78 values of 0xf0 through 0xf3 (binary 111100xx).
   Any OS image starts at page 0 of flash device 0, or page 0 of flash device 1 if there are two flash devices on board.
   I/O port 0x78 is defined as follows:
   Bits 4 - 7:Page Number
   Bits 2 - 3:Flash Device
   Bit 1:0 = Flash write disabled, 1= Flash write enable.
   Bit 0: Varies; should always be written back with the same value that was read.
   Mechanism 2:
   The BIOS starts in page 0 and may grow into subsequent pages. The flash OS, if loaded, starts in the highest numbered page and grows into lower number pages as necessary.
   The I/O port 0x78 is defined as follows:
   Bit 7:0 = Flash write disabled, 1= Flash write enable.
   Bits 3 – 0: Page number
   Mechanism 3:
   Flash is not paged.
   I/O port 0xe4 is defined as follows:
   Bit 5: 0 = flash write disabled, 1= flash write enable.
   Other Bits: Reserved; should always be written back with the same value that was read
6. The version numbers are changed when one or more elements are added to the structure. The offsets to the existing elements always remain the same. All new elements are appended to the existing elements and must be naturally aligned.
7. The checksumPad is used when a BIOS image is changed. The 8-bit checksum of the whole image has to be recalculated. The sum of all the bytes in an image should always equal zero.
8. The NetworkIDPad is used when a BIOS network ID is programmed into an image. The 8-bit checksum of the six bytes of network ID plus the NetworkIDPad should always equal zero.

9. All 32-bit address fields indicate the absolute physical address of the beginning of the given area. For mechanisms that use paging, the address is valid only when the corresponding page has been selected. Any given area may be large enough that it extends past the flash page where it starts. In such a case, it is the responsibility of the programmer to calculate the additional page(s) that need to be selected, as well as the offsets into the page(s).
If an area of flash is decoded at more than one address range, the address value given in the table is the address where the flash image should be programmed. For example, a 256 KB BIOS area using Mechanism 1 would be listed in the paged area at 0xfff80000, page 15. It would not be listed at 0xfffc0000, which might contain either the flash BIOS or a FRED device.
The value of an address field and its corresponding page field are undefined if the corresponding size field is zero. For example, if the BootBlockSize field is zero, then the values in BootBlockAddr and BootBlockPage are invalid, and whatever memory space they point to should not be accessed. In this case, the “first” block of the flash drive is actually at the top of the flash drive address space, directly below the BIOS and other related areas. The flash drive area normally grows downward, starting at this block, and the logical blocks of the flash drive are normally numbered with this block as block zero.
The bottom of the flash drive address space is calculated by taking the ending address of this block, subtracting the size of the flash drive, and then performing any necessary paging calculations.

How to Find the System Information Structure

The dynamic version of the System Information Structure can be found by searching the BIOS area (F000:0000h - F000:FFFFh in real mode). The following C function is an example of how to find the structure.

```
#define SIGNATURE “ZIA INFO”
#define SigSIZE8
ZiaSysInfo *infoptr;
/*----------------------------------------------------------------------
* GetSysInfo
*
*This function searches the BIOS area(f000h - fffff) for
*the system information structure. The structure starts with
*signature "ZIA INFO. Once it is found, the global structure
*pointer "infoptr" is loaded to point to the structure.
*
*Input:
*None
*
*Output:
*return 0 if the structure is found
*return 1 if the structure is NOT found
*-----------------------------------------------------------------------*/
UNIT8 GetSysInfo(void)
{
UINT16 i=0;
UINT8 __far *ptr;
_FP_SEG(ptr) = 0xf000;
_FP_OFF(ptr) = 0;
for (i=0; i<(0xffff-SigSIZE); i++) {
if (strncmp((ptr+i),SIGNATURE,SigSIZE)==0){
_FP_SEG(infoptr) = 0xf000;
_FP_OFF(infoptr) = i;
return(0);
}
}
```

```
return(1);
}
```

It is the application's responsibility to check and account for the size and version of the structure. The structure is designed so that any additions or changes are backward compatible: additional fields are added at the end, so that the rest of the structure has the same organization as the previous version.

9.4 OSFlash

OSFlash (also known as FlashOS) is an additional boot source that appears as a device in the boot order menu. The boot source consists of a user-supplied image stored in flash memory, which is copied into RAM by the BIOS and then executed. The function and purpose of the boot image is completely up to the user.

Implementation

The OSFlash image is stored at the bottom of the flash memory space on the board. Exactly what constitutes the "bottom" depends on the flash configuration of the platform, and may be somewhat arbitrary on a board with a paged flash area.

The boot image in flash is preceded by a header that defines the load and entry points:

```
struct {
UINT8 sig[16]; /* signature: 'ALTERNATE OS mr' */
INT32 dest; /* 32-bit flat address where image is */
/* copied to RAM default 800h */
UINT32 entry; /* segment/offset of execution entry point */
/* image, default 80:0h */
UINT16 blocks; /* number of 64K blocks to copy when loading */
/* image into RAM */
UINT16 last; /* number of 16 bit WORDS to copy in last */
/* block (range 1-8000h) */
UINT32 image_size;/* total image size in bytes (not currently */
/* used by loader) */
} os_header;
As an example, an image of size 94F01h, which should be loaded at 1000h
and entered at 100:80h (absolute address 1080h), would have these values in
the header:
dest = 0x1000;
entry = (0x100 << 16 ) | 0x80);
blocks = 0xA;
last = 0x2781; /* 0x4F01 divided by two and rounded up */
image_size = 0x94F01;
```

9.5 Plug and Play (PnP)

The system BIOS supports the following industry standards for making the system "Plug and Play ready" such as ACPI, PCI local bus specification rev 2.1 and SMBIOS 1.

Resource Allocation

The system BIOS identifies, allocates, and initializes resources in a manner consistent with other Performance Technologies servers. The BIOS scans, in order, for the following:

ISA devices: *Add-in ISA devices are not supported on this platform.* However, some standard PC peripherals may require ISA-style resources – resources for these devices are reserved as needed.

Add-in video graphics adapter (VGA) devices: If found, the BIOS initializes and allocates resources to these devices.

PCI Devices: The BIOS allocates resources according to the parameters set up by the SSU and as required by the *PCI Local Bus Specification*, Revision 2.1.

The system BIOS Power-on Self Test (POST) guarantees that there are no resource conflicts prior to booting the system. Please note that PCI device drivers are required to support the sharing of IRQs. Sharing IRQs should not be considered a resource conflict. Note that only four legacy IRQs are available for use by PCI devices; as a result, most of the PCI devices share legacy IRQs. In SMP mode, the I/O APICs are used instead of the legacy “8259-style” interrupt controller. There is very little interrupt sharing in SMP mode.

PnP ISA Auto-Configuration

The system BIOS:

- Supports relevant portions of the *Plug and Play ISA Specification*, Revision 1.0a and the *Plug and Play BIOS Specification*, Revision 1.0A.
- Assigns I/O, memory, direct memory access (DMA) channels, and IRQs from the system resource pool to the embedded PnP Super I/O device.
- Does *not* support add-in PnP ISA devices.

PCI Auto-Configuration

The system BIOS supports the INT 1Ah, AH = B1h functions, in conformance with the *PCI Local Bus Specification*, Revision 2.1. The system BIOS also supports the 16 and 32-bit protected mode interfaces as required by the *PCI BIOS Specification*, *Revision 2.1*.

Beginning at the lowest device, the BIOS uses a “depth-first” scan algorithm to enumerate the PCI buses. Each time a bridge device is located, the bus number is incremented and scanning continues on the secondary side of the bridge before all devices are scanned on the current bus. The BIOS then scans for PCI devices using a “breadth-first” search – all devices on a given bus are scanned from lowest to highest before the next bus number is scanned.

System BIOS POST maps each device into memory and/or I/O space, and assigns IRQ channels as required. The BIOS programs the PCI-ISA interrupt routing logic in the chipset hardware to steer PCI interrupts to compatible ISA IRQs.

The BIOS dispatches any option ROM code for PCI devices to the DOS compatibility hole (C0000h to DFFFFh) and transfers control to the entry point. The DOS compatibility hole is a limited resource, so system configurations with a large number of PCI devices may result in a shortage of this resource. If the BIOS runs out of option ROM space, some PCI option ROMs are not executed and a POST error is generated. Scanning PCI option ROMs may be controlled on a slot-by-slot basis in the BIOS setup.

Drivers and/or the OS can detect the installed devices and determine resource consumption using the defined PCI, legacy PnP BIOS, and/or ACPI BIOS interface functions.

Legacy ISA Configuration

Legacy ISA add-in devices are not supported by these platforms.

Automatic Detection of Video Adapters

The BIOS detects video adapters in the following order:

Offboard PCI

Onboard PCI

The onboard (or offboard) video BIOS is shadowed, starting at address C0000h, and is initialized before memory tests begin in POST. Precedence is always given to offboard devices.

9.6 BIOS Recovery

If the system fails to complete POST and boot an operating system, the BMC switches to the backup BIOS (in flash) to boot, then the runtime BIOS (in flash) can be re-programmed with the flash utility.

9.7 Console Redirection

Console redirection allows users to monitor the ZT 5515*e*'s boot process and to run the ZT 5515*e*'s Setup utility from a remote serial terminal. Connection is made either directly through a serial port or through a modem.

The console redirection feature is most useful in cases where it is necessary to communicate with a processor board, such as the ZT 5515*e*, in an embedded application without video support.

The BIOS supports redirection of both video and keyboard via a serial link (COM 1 or COM 2). When console redirection is enabled in BIOS setup, local (host server) keyboard input and video output are passed both to the local keyboard and video connections, and to the remote console via the serial link. Keyboard inputs from both sources are considered valid and video is displayed to both outputs. Optionally, the system can be operated without a host keyboard or monitor attached to the system and run entirely via the remote console. Setup and any other text-based utilities can be accessed via console redirection.

9.8 System Management BIOS (SMBIOS)

The ZT 5515*e* follows the criteria outlined in the *System Management BIOS Reference Specification, Version 2.3*. Refer to this specification for details on SMBIOS.

Section
10 Specifications

This section describes the electrical, environmental, and mechanical specifications of the ZT 5515*e*. It includes connector descriptions and pinouts, as well as illustrations of the board dimensions and connector locations.

10.1 Electrical and Environmental

The topics listed below provide tables and illustrations showing the following electrical and environmental specifications:

- Absolute maximum ratings
- DC operating characteristics
- Battery backup characteristics

Absolute Maximum Ratings

The values below are stress ratings only. Do not operate the ZT 5515*e* at these maximums. See the "DC Operating Characteristics" topic in this section for operating conditions.

Supply Voltage, Vcc:	6.5V
Supply Voltage, Vcc3:	4.5V
Supply Voltage, AUX +:	15V
Supply Voltage, AUX -:	-15V
Storage Temperature (no hard disk):	-40° to +85° Celsius
Storage Temperature (with hard disk):	-40° to +65° Celsius
Non-Condensing Relative Humidity:	<95% at 40° Celsius

DC Operating Characteristics

Supply Voltage, Vcc:	4.85V minimum to 5.25V maximum
Supply Voltage, Vcc3:	3.20V minimum to 3.47V maximum
Supply Voltage, AUX +:	10.8V minimum to 13.2V maximum

Supply Voltage, AUX -:	-13.2V minimum to -10.8V maximum
Supply Current, Icc:	4.5A average (typical with 1.2 GHz processor and 512 MB SDRAM. Peak (short duration) power supply current may be significantly higher (up to 50%) and may vary depending upon the application.
Supply Current, Icc3:	2.5A average (typical with 1.2 GHz processor and 512 MB SDRAM. Peak (short duration) power supply current may be significantly higher (up to 50%) and may vary depending upon the application.
Supply Current, AUX + (12V):	50mA maximum

Battery Backup Characteristics

Battery Voltage:	3V
Battery Capacity:	250mAh
Real-Time Clock Requirements:	8μA maximum (Vbat = 3V, Vcc=0V)
Real-Time Clock Data Retention:	31,250 hours / 3.7 years minimum (not powered); 5.2 years minimum (with Vcc power applied 8 hours per day)
Electrochemical Construction:	Long life lithium with solid-state polycarbon monofluoride cathode.

CAUTION: The ZT 5515*e* contains a lithium battery. This battery is not field-replaceable. There is a danger of explosion if the battery is incorrectly replaced or handled. Do not disassemble or recharge the battery. Do not dispose of the battery in fire. When the battery is replaced, the same type or an equivalent type recommended by the manufacturer must be used. Used batteries must be disposed of according to the manufacturer's instructions. Return the board to Performance Technologies for battery service.

Operating Temperature

The ZT 5515*e*'s heatsink allows a maximum ambient air temperature of 50°C with 200 LFM (linear feet per minute) of airflow. External airflow *must* be provided to the ZT 5515*e* at all times. Refer to the "Electrical and Environmental" topic in Section 2 for additional information. Also refer to the topic "Temperature Monitoring" in Section 11 for details on monitoring the processor temperature.

10.2 Reliability

MTBF: 23.6 years (excluding on-board hard disk drive)

MTTR: 3 minutes (based on board replacement), plus system startup

10.3 Mechanical

This section includes the following mechanical specifications:

- Dimensions and weight
- Connector locations, descriptions, and pinouts

Board Dimensions and Weight

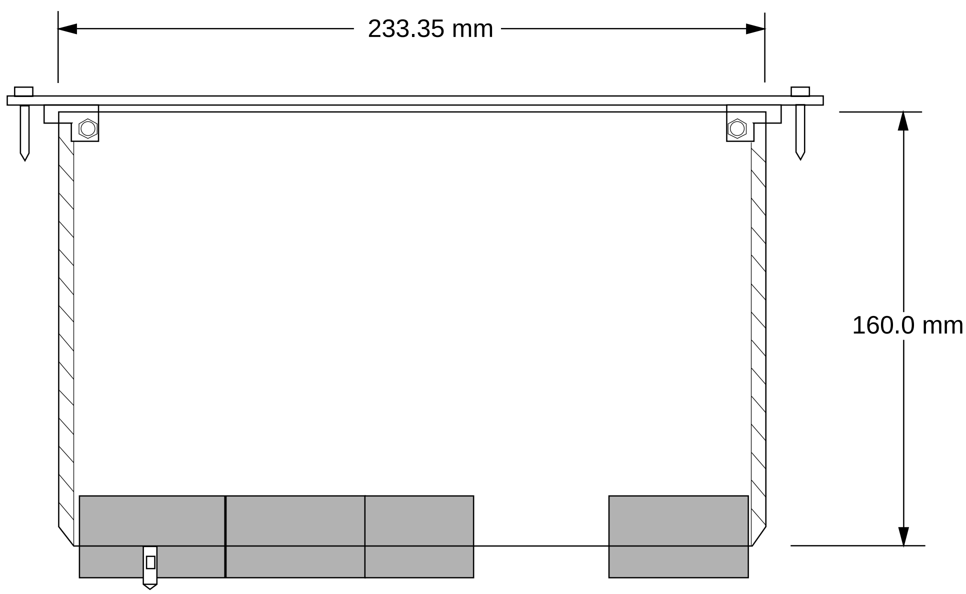
The ZT 5515*e* meets the *CompactPCI Specification, PICMG 2.0, Version 2.1* for all mechanical parameters. Mechanical dimensions are shown in the "PCB Dimensions" illustration and are outlined below.

PCB Dimensions: 233.35 mm x 160 mm x 1.6 mm

Board Dimensions: 6U x 4HP (one slot)

Weight: 509 grams (18 ounces) with processor, heatsink, 512MB memory

Figure 10. PCB Dimensions



Connectors

The ZT 5515*e* includes several connectors to interface to application-specific devices. A detailed description and pinout for each connector is given in Section 4, "Connectors."

Section

11 Thermal Considerations

This section describes the thermal requirements for reliable operation of a ZT 5515*e* using the Mobile Intel Pentium 4 processor - M. It covers basic thermal requirements and provides specifics about monitoring the board and processor temperature.

11.1 Thermal Requirements

The ZT 5515*e* is equipped with an integrated heatsink for cooling the processor module. The maximum processor core temperature ***must not exceed 100°C***. The heatsink allows a maximum ambient air temperature of 50°C with 200 linear feet per minute (LFM) of airflow. The maximum power dissipation of the CPU is 25 W at 1.2GHz and 1.20V.

CAUTION: External airflow must be provided at all times during operation to avoid damaging the CPU. Performance Technologies strongly recommends the use of a fan tray below the card rack to supply the external airflow.

The "Thermal Requirements" table below shows the relationship between ambient air temperature, board temperature, and processor core temperature.

Table 19. Thermal Requirements

External Ambient Air Temperature (°C)	Temperature Around the Board (°C)	Pentium 4 processor Core Temperature (°C)
0	13	44
5	18	49
10	22	54
15	27	60
20	33	65
25	37	69
30	42	74
35	47	79
40	52	84
45	57	89
50	63	95
55	68	100 = maximum

11.2 Temperature Monitoring

Because reliable long-term operation of the ZT 5515*e* depends on maintaining proper temperature, Performance Technologies strongly recommends verifying the operating temperature of the processor module and processor core in the final system configuration.

The Pentium 4 processor incorporates an on-die thermal diode that can be used to monitor the processor's die temperature. The ZT 5515*e* includes an AMD 1026 hardware monitor to check the die temperature of the processor for thermal management purposes.

When checking airflow conditions, let the processor core temperature test dwell for at least 30 minutes and verify that the core temperature does not exceed 65°C. The processor "core" temperature must **never** exceed 100°C under any condition of ambient temperature or usage.

Caution: Temperatures over 100°C may result in permanent damage to the processor.

Refer to the "Thermal Requirements" table for more information.

Section
12 System Registers

The ZT 5515*e* provides several system registers to control and monitor a variety of functions. Normally, only the system BIOS uses these registers, but they are documented here for application use as needed. Take care when modifying the contents of these registers: the system BIOS may be relying on the state of some bits.

12.1 System Register Definitions

The System Registers are accessible as follows:

	I/O Address	Register Name	Default Value	Access	Size
PAL	78h	Flash Control	0x00	R/W	8 bits
	79h	Watchdog	0x00	R/W	8 bits
	7Bh	PAL Revision ID	0x00	R/W	8 bits
	80h	Port 80 BIOS Post Codes	0x00	WO	8 bits
	E3h	Switch Monitors	0x00	RO	8 bits
	E4h	Geographic Addressing	0x00	RO	8 bits
	E6h	J1 SMBus Enable	0x00	WO	8 bits

Flash Control (78h)

I/O Address: 78h

Default Value: 0x00

Size: 8 bits

Attribute: R/W

NOTE: This register is reset to 00h on init or reset. The BIOS resides in page 000.

Bit	Description	Default
7	**Flash Write Protection** Controls Write Enable to flash: 0 = Write protects flash 1 = Allows writes to flash Flash memory is discussed in Section 9, “System BIOS.”	0
6:4	**RESERVED**	0
3	**Page 3** Flash A23 (1MB page)	0
2	**Page 2** Flash A22 (1MB page)	0
1	**Page 1** Flash A21 (1MB page)	0
0	**Page 0** Flash A20 (1MB page)	0

Watchdog (79h)

I/O Address: 79h

Default Value: 0x00

Attribute: R/W

Bit	Description
7	**Stage 2 Monitor (Reset Monitor)** Monitors the second stage (Reset) timer status. Read Value: 0 = Watchdog has not timed out since power up or since this bit was last set to 0. 1 = Watchdog reset timeout occurred since power up or since bit was last set to 0. Write Value: 0 = Sets this bit to 0. 1 = No effect. Power Up Value = 0. A hard reset not caused by a watchdog timeout sets this bit to 0.
6	**Stage 1 Monitor (NMI or INIT Monitor)** Monitors the first stage (NMI or INIT) timer status. Read Value: 0 = Watchdog has not timed out since power up or since this bit was last set to 0; 1 = Watchdog timed out and either: • NMI output was asserted if bit 3 = 0; or • INIT output was asserted if bit 3 = 1. Write Value: 0 = Sets this bit to 0. 1 = No effect. Power Up Value = 0. A hard reset sets this bit to 0.

Watchdog (79h), continued

Bit	Description
3	**NMI or INIT** Selects between generating an NMI or a CPU INIT. Read Value: 0 = NMI 1 = INIT This bit is set to 0 at reset. Write Value: 0 = NMI is generated when the watchdog times out. 1 = INIT is generated when the watchdog times out. Power Up Value = 0. A hard reset sets this bit to 0.
2:0	**Terminal Count (TermCnt2…TermCnt0)** Read Value: Reflects the value written to bits 2 through 0. Write Value: These bits determine the terminal count of the watchdog. Below is the minimum timeout period. The watchdog times out in no less than the minimum value. The nominal timeout period is 30% longer than the minimum. 000 = 250 ms 100 = 32 s 001 = 500 ms 101 = 64 s 010 = 1 s 110 = 128 s 011 = 8 s 111 = 256 s Power Up Value = 000. A hard reset sets these bits to 000.

PAL Revision ID (7Bh)

I/O Address: 7Bh

Default Value: 0x00

Attribute: R/W

Bit	Description
7:4	**Reserved**
3:0	**Reserved (PAL ID)**

Port 80 BIOS POST Codes (80h)

I/O Address: 80h

Default Value: 0x00

Size: 8 bits

Attribute: WO

Bit	Description
7:0	**D7-D0** These bits correspond to eight LEDs (labeled D0 through D7) on the solder side of the PCB. The Port 80 bits report the BIOS POST (diagnostic) codes. These LEDS may not be visible if a hot swap shield is installed on the board. D7 corresponds to the most significant bit.

Switch Monitors (E3h)

Address Offset: E3h

Default Value: 0x80

Size: 8 bits

Attribute: RO

Bit	Description
7	**Flash Write-Protect Status** This bit corresponds to the status of switch SW2-1. 0 = Flash is write-protected by SW2-1 1 = Flash is *not* write-protected by SW2-1
6	**System Enable** This bit corresponds to the status of SYSEN. 0 = ZT 5515e is plugged into a peripheral slot 1 = ZT 5515e is plugged into a system slot
5	**Boot Source Selection** This bit indicates the switch setting of boot block page selection. 0 = Protected page (Top page) 1 = Top page -1
4	**Manufacturing Mode** This bit is used during production testing to load a default CMOS image. 0 = non-manufacturing mode 1 = manufacturing mode
3	**Reserved**
2	**Console Redirection Enable** This bit reads the status of switch SW4-3. 0 = SW4-3 is open and console redirection is not enabled 1 = SW4-3 is closed and console redirection is enabled Refer to the "Console Redirection" section in the *Performance Technologies Embedded BIOS Manual* before attempting to use this feature.
1:0	**Software Configuration** These bits are used to provide configuration information to the user's software by monitoring the status of the software configuration SW4 segments listed below. An open switch reads back a 0; a closed switch reads back a 1. The bits correspond to switch segments as follows: **Bit 0** = SW4-1; **Bit 1** = SW4-2; **Bit 2** = SW4-3

Geographic Addressing (E4h)

Address Offset: E4h

Default Value: 0x00

Size: 8 bits

Attribute: RO

Bit	Description
7:6	**Reserved**
5	**Ethernet Channel A Front/Rear panel Switching** This bit controls the MUX used to switch Ethernet channel A between the front and rear panel. 0 = Front panel selected 1 = Rear panel selected The power up default is 0. This is also a BIOS selectable option.
4:0	**Geographic Addressing** CompactPCI defines several signal additions to the PCI specification. One of these is GA[4..0], used for geographic addressing on the backplane. Geographic addressing uniquely differentiates each board based upon the physical slot into which it was inserted. Each backplane connector in a CompactPCI system has a unique code for GA[4..0]. See the *CompactPCI Specification, PICMG 2.0, Version 2.1* for more information on geographic addressing. The bits correspond to signals as follows: **Bit 0** = GA0; **Bit 1** = GA1; **Bit 2** = GA2; **Bit 3** = GA3; **Bit 4** = GA4. 0 = The corresponding GA pin is open. 1 = The corresponding GA pin is low (GND)

SMBus Enable (E6h)

Address Offset: E6h

Default Value: 0x00

Size: 8 bits

Attribute: R/W

Bit	Description
7	**Reserved**
6	**J1 SMBus Enable** This bit enables SMBus function through the rear panel J1 connector. 0 = J1 SMBus disabled 1 = J1 SMBus enabled
5	**Rear Panel NMI Status** 0 = An NMI was not asserted by the rear panel 1 = An NMI was asserted by the rear panel Users can write a 0 to clear this bit.
4:0	**Reserved**

Section
13 Datasheet Reference

This section provides links to datasheets, standards, and specifications for the technology designed into the ZT 5515*e*.

13.1 CompactPCI

CompactPCI specifications can be purchased from the PCI Industrial Computer Manufacturers Group (PICMG) for a nominal fee. A short form CompactPCI specification is also available on PICMG's Web site at:

http://www.picmg.org

13.2 Ethernet

Refer to the Intel *82546EB Dual Port Gigabit Ethernet Controller* datasheet for more information on the Ethernet LAN Controller. The datasheet is available from Intel's Web site at:

http://developer.intel.com/design/network/products/lan/controllers/82546.htm

13.3 Intel 845E Chipset

For more information on the following ZT 5515*e* functions, refer to the *Intel 845E* datasheet.

- USB
- Counter/timers
- DMA controllers
- Real-time clock
- Interrupt controllers
- Reset control register
- IDE interface controller

This datasheet and other information are available online at:

http://developer.intel.com/design/chipsets/embedded/251335.htm

13.4 Mobile Intel Pentium 4 Processor - M (FCPGA Package)

For more information about the Intel Mobile Pentium 4 Processor - M in FCPGA Package, see the *Mobile Intel Pentium 4 processor - M in FCPGA* datasheet. This document is available online at:

http://developer.intel.com/design/mobile/pentium4p-m/p4p-m.htm

13.5 PMC Specification

For more information about PMC modules and the PMC Specification, refer to the sponsoring organization's Web site at:

http://www.vita.com/

13.6 SuperI/O

Refer to the National Semiconductor *PC87417 SuperI/O Plug and Play Compatible Chip in Compact 100-Pin VLJ Packaging* datasheet for more information on the following ZT 5515*e* functions:

- Floppy disk controller
- Serial port controller
- Mouse and keyboard controller

The datasheet is available online from the National Semiconductor Web site at:

http://www.national.com/pf/PC/PC87417.html#Datasheet

13.7 User Documentation

The latest product information and manuals are available on the Performance Technologies Web site at http://www.pt.com.

13.8 Video

For the latest Silicon Motion LynxEM+ drivers, refer to the Silicon Motion Web site at:

http://www.siliconmotion.com/en/driverslist.htm

Section

14 Agency Approvals

14.1 CE Certification

The ZT 5515*e* meets the intent of Directive 89/336/EEC for Electromagnetic Compatibility and Low-Voltage Directive 73/23/EEC for Product Safety. The ZT 5515*e* has been designed for NEBS/ETSI compliance.

14.2 Safety

UL/cUL 60950	Safety for Information Technology Equipment (UL File # E139737)
EN/IEC 60950	Safety for Information Technology Equipment
CB Report Scheme	CB certificate and Report

14.3 Emissions Test Regulations

FCC Part 15, Subpart B

EN 55022

CISPR 22

Bellcore GR-1089

EN 50081-1 Emissions

GR-1089-CORE	Sections 2 and 3
EN 55022	Class A Radiated
EN 55022	Power Line Conducted Emissions
EN 61000-3-2	Power Line Harmonic Emissions
EN 61000-3-3	Power Line Fluctuation and Flicker

EN 55024 Immunity

GR-1089-CORE	Sections 2 and 3
EN 61000 4-2	Electro-Static Discharge (ESD)
EN 61000 4-3	Radiated Susceptibility

EN 61000 4-4	Electrical Fast Transient Burst
EN 61000 4-5	Power Line Surge
EN 61000 4-6	Frequency Magnetic Fields
EN 61000 4-11	Voltage Dips, Variations, and Short Interruptions

14.4 Regulatory Information

FCC (USA)

This product has been tested and found to comply with the limits for a Class A digital device pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment.

This product generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

NOTE: This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference.
2. This device must accept any interference received, including interference that may cause undesired operation.

Caution: If you make any modification to the equipment not expressly approved by Performance Technologies, you could void your authority to operate the equipment.

14.5 Industry Canada (Canada)

Cet appareil numérique respecte les limites bruits radioélectriques applicables aux appareils numériques de Classe A prescrites dans la norme sur le matériel brouilleur: “Appareils Numériques,” NMB-003 édictée par le Ministre Canadien des Communications.

This digital apparatus does not exceed the Class A limits for radio noise emissions from digital apparatus set out in the interference-causing equipment standard entitled: “Digital Apparatus,” ICES-003 of the Canadian Department of Communications.

Section

15 In Case of Difficulty

If you encounter difficulty in using this Performance Technologies product, you can contact our support personnel in several ways. Please have the product model and serial number handy before contacting Product Support.

Internet

www.pt.com

Email

support@pt.com

Describe your problem in detail. Please include your return email address and telephone number.

FAX

(805) 541-5088

Mark your FAX “Attention: Product Support.” Describe your problem in detail. Please include your return FAX number and telephone number.

Telephone

(805) 541-0488

Request Product Support. Our offices are open between 8:00 am and 5:00 pm Pacific Time, Monday through Friday.

If you are located outside North America, we encourage you to contact the local Performance Technologies distributor or agent for support. Many of our distributors or agents maintain technical support staffs.

Performance Technologies
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